Preliminary data sheet

LH7A400
32-Bit System-on-Chip

FEATURES

- 32-bit ARM9TDMI™ RISC Core
  - 16 kB Cache: 8 kB Instruction and 8 kB Data
  - MMU (Windows CE™ Enabled)
  - Up to 250 MHz; see Table 1 for options
- 80 kB On-Chip Static RAM
- Programmable Interrupt Controller
- External Bus Interface
  - Up to 125 MHz; see Table 1 for options
  - Asynchronous SRAM/ROM/Flash
  - Synchronous DRAM/Flash
  - PCMCIA
  - CompactFlash
- Clock and Power Management
  - 32.768 kHz and 14.7456 MHz Oscillators
  - Programmable PLL
- Programmable LCD Controller
  - Up to 1,024 × 768 Resolution
  - Supports STN, Color STN, AD-TFT, HR-TFT, TFT
  - Up to 64 k-Colors and 15 Gray Shades
- DMA (10 Channels)
  - AC97
  - MMC
  - USB
- USB Device Interface (USB 2.0, Full Speed)
- Synchronous Serial Port (SSP)
  - Motorola SPI™
  - Texas Instruments SSI
  - National MICROWIRE™
- Three Programmable Timers
- Three UARTs
  - Classic IrDA (115 kbit/s)
- Smart Card Interface (ISO7816)
- Two DC-to-DC Converters
- MultiMediaCard™ Interface
- AC97 Codec Interface
- Smart Battery Monitor Interface
- Real Time Clock (RTC)
- Up to 60 General Purpose I/Os
- Watchdog Timer
- JTAG Debug Interface and Boundary Scan
- Operating Voltage
  - 1.8 V Core
  - 3.3 V Input/Output
- 5 V Tolerant Digital Inputs (except oscillator pins)
  - Oscillator pins P15, P16, R13, and T13 are 1.8 V ± 10 %.
- Operating Temperature: –40°C to +85°C
- 256-ball BGA or 256-ball LFBGA Package

DESCRIPTION

The LH7A400, powered by an ARM922T, is a complete System-on-Chip with a high level of integration to satisfy a wide range of requirements and expectations.

This high degree of integration lowers overall system costs, reduces development cycle time and accelerates product introduction.

Table 1. LH7A400 versions

PART NUMBER	CORE CLOCK	BUS CLOCK	LOW POWER CURRENT BY MODE (TYP.)	TEMP. RANGE
LH7A400N0F076B5	250 MHz/ 245 MHz	125 MHz	Run = 250 mA; Halt = 50 mA; Standby = 129 µA	0°C to +70°C/ –40°C to +85°C
LH7A400N0F000B3A	200 MHz/ 195 MHz	100 MHz	Run = 125 mA; Halt: 25 mA; Standby = 42 µA	0°C to +70°C/ –40°C to +85°C
LH7A400N0F000B5	200 MHz/ 195 MHz	100 MHz	Run = 125 mA; Halt: 25 mA; Standby = 42 µA	0°C to +70°C/ –40°C to +85°C
LH7A400N0G000B5	200 MHz/ 195 MHz	100 MHz	Run = 125 mA; Halt: 25 mA; Standby = 42 µA	0°C to +70°C/ –40°C to +85°C

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
LH7A400N0G000B5	BGA256	plastic ball grid array package; 256 balls	SOT1018-1
LH7A400N0F000B3A	LFBGA256	plastic low profile fine-pitch ball grid array package; 256 balls	SOT1020-1
LH7A400N0F000B5	LFBGA256	plastic low profile fine-pitch ball grid array package; 256 balls	SOT1020-1
LH7A400N0F076B5	LFBGA256	plastic low profile fine-pitch ball grid array package; 256 balls	SOT1020-1

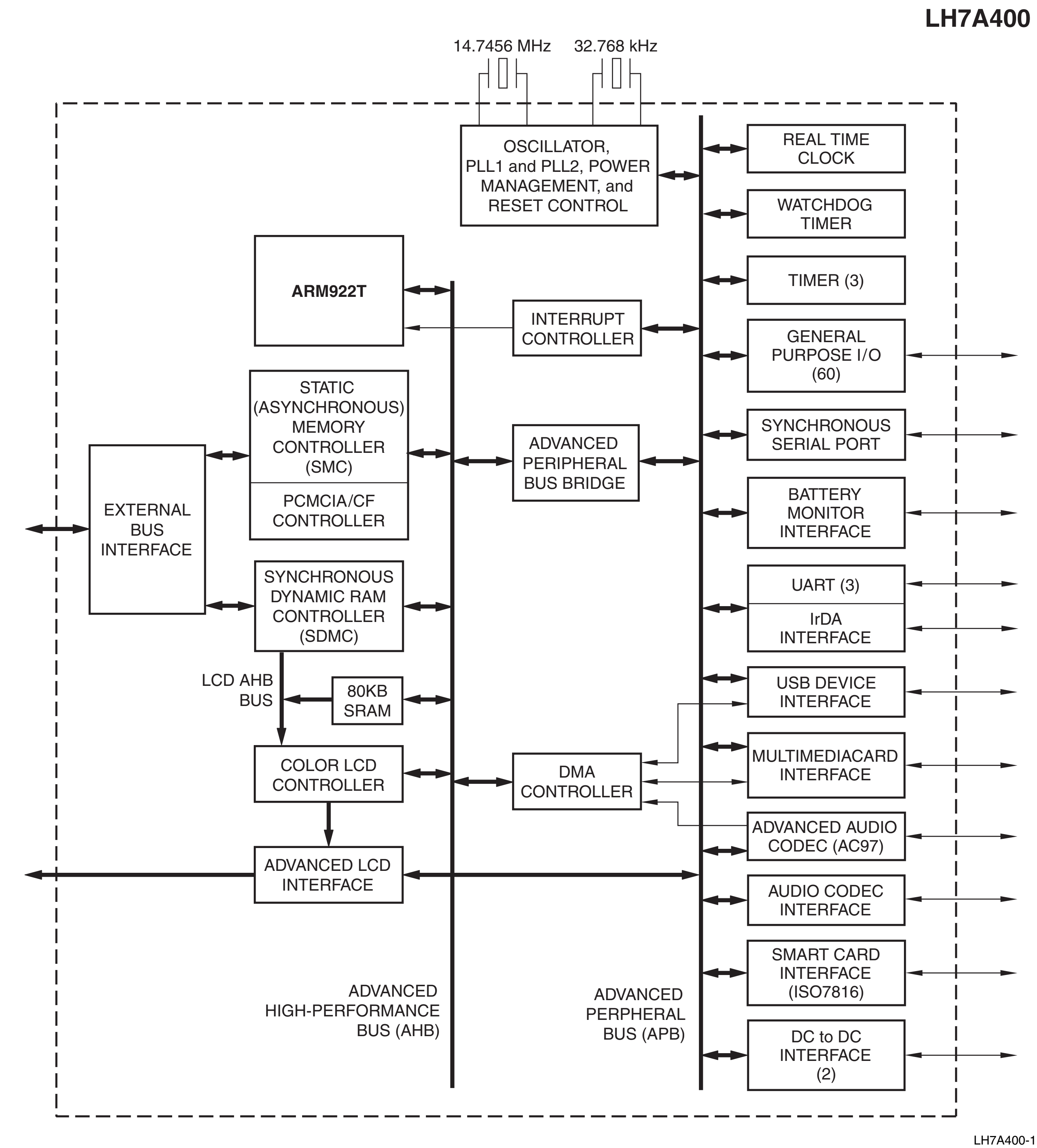


Figure 1. LH7A400 block diagram

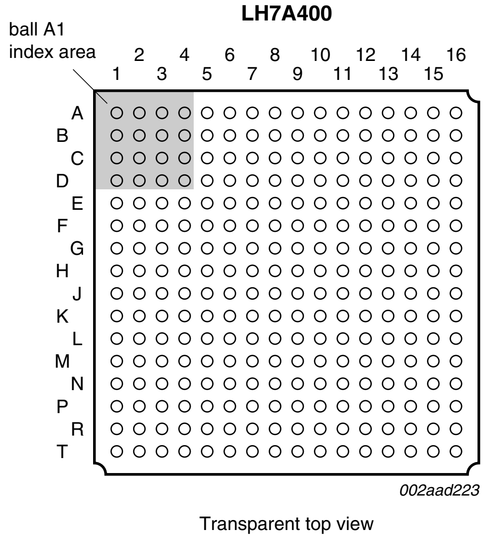


Figure 2. Pin configuration (BGA256)

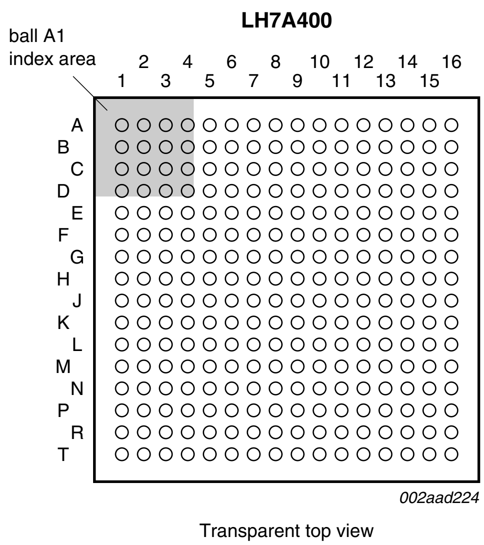


Figure 3. Pin configuration (LFBGA256)

Table 3. Functional Pin List

BGA PIN	LFBGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
G7	C10	VDD	I/O Ring Power					
F1	F9							
K7	F11							
M1	F14							
M5	G8							
T6	H13							
R14	J9							
M14	K15							
J11	L7							
J12	N6							
F13	N8							
B14	N12							
E10	N13							
B8	P11							
H7	B8	VSS	I/O Ring Ground					
G3	C6							
K4	D5							
N5	D13							
P6	E8							
T14	F7							
R16	G13							
N16	H9							
K13	J14							
H9	K7							
C15	L8							
A11	L10							
E8	L12							
A5	M11							
F7	M14							
E1	C4	VDDC	Core Power					
J4	D7							
P3	D10							
T8	F4							
K9	F10							
L13	J4							
E15	J8							
D12	K8							
A7	L6							
H5	G7	VSSC	Core Ground					
M3	H4							
L9	H8							
T10	L4							
N15	L9							
H12	N3							
B15	N7							
C9	N10							
G6	R5							

Table 3. Functional Pin List (Cont'd)

BGA PIN	LFBGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
R11	P12	VDDA	Analog Power for PLL					
N12	M10							
P12	R13	VSSA	Analog Ground for PLL					
T11	N11							
D3	E4	nPOR	Power On Reset	Input	No Change		I	3
H6	D1	nURESET	User Reset; should be pulled HIGH for normal or JTAG operation.	Input	No Change		I	3
D4	E2	WAKEUP	Wake Up	Input	No Change		I	3
E4	F2	nPWRFL	Power Fail Signal	Input	No Change		I	3
C2	D2	nEXTPWR	External Power	Input	No Change		I	3
R13	R14	XTALIN	14.7456 MHz Crystal Oscillator pins. An external clock source can be connected to XTALIN leaving XTALOUT open.	Input	No Change		I	
T13	R15	XTALOUT		HIGH	HIGH		O	
P16	N14	XTAL32IN	32.768 kHz Real Time Clock Crystal Oscillator pins. An external clock source can be connected to XTAL32IN leaving XTAL32OUT open.	Input	No Change		I	
P15	M13	XTAL32OUT		Output	No Change		O	
P14	M12	CLKEN	External Osc Clock Enable Output	LOW	LOW	8 mA	O	
J6	J5	PGMCLK	Programmable Clock (14.7456 MHz MAX.)	LOW	LOW or HIGH	8 mA	O	
K11	P14	nCS0	Async Memory Chip Select 0	HIGH	No Change	12 mA	O	
K10	P16	nCS1	Async Memory Chip Select 1	HIGH	No Change	12 mA	O	
P13	N15	nCS2	Async Memory Chip Select 2	HIGH	No Change	12 mA	O	
M12	N16	nCS3/ nMMSPICS	• Async Memory Chip Select 3 • MultiMediaCard SPI Mode Chip Select	HIGH: nCS3	No Change	12 mA	O	
L12	L11	D0	Data Bus	LOW	LOW	12 mA	I/O	
M15	L13	D1						
N13	L14	D2						
L16	K11	D3						
L15	L16	D4						
L14	K14	D5						
H11	J15	D6						
K12	J12	D7						
J15	J10	D8						
J13	H16	D9						
J10	H14	D10						
H15	H11	D11						
H13	G16	D12						
G15	G9	D13						
G11	G14	D14						
G12	G12	D15						
F15	F15	D16						
F12	E15	D17						
E14	D16	D18						
D16	F12	D19						
H10	E13	D20						
D14	D14	D21						
F10	E12	D22						
A16	B16	D23						
A14	D12	D24						
B13	A16	D25						

Table 3. Functional Pin List (Cont'd)

BGA PIN	LFBGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
C13	B13	D26	Data Bus	LOW	LOW	12 mA	I/O	
E12	B14	D27						
G10	C12	D28						
B12	A14	D29						
B11	B12	D30						
D11	A12	D31						
M16	M15	A0/nWE1	• Asynchronous Address Bus • Asynchronous Memory Write Byte Enable 1	HIGH: nWE1	HIGH	12 mA	O	
N14	M16	A1/nWE2	• Asynchronous Address Bus • Asynchronous Memory Write Byte Enable 2	HIGH: nWE2	HIGH	12 mA	O	
M13	L15	A2/SA0	• Asynchronous Address Bus • Synchronous Address Bus	LOW	LOW	12 mA	O	
K16	K12	A3/SA1						
K15	K13	A4/SA2						
K14	K16	A5/SA3						
J8	J13	A6/SA4						
J16	J11	A7/SA5						
J14	J16	A8/SA6						
J9	H15	A9/SA7						
H16	H10	A10/SA8						
H14	H12	A11/SA9						
G16	G15	A12/SA10						
G14	G10	A13/SA11						
G13	G11	A14/SA12						
F16	F16	A15/SA13						
F14	E16	A16/SB0	• Async Address Bus • Sync Device Bank Address 0	LOW	LOW	12 mA	O	
E16	F13	A17/SB1	• Async Address Bus • Sync Device Bank Address 1	LOW	LOW	12 mA	O	
E13	E14	A18	Asynchronous Address Bus	LOW	LOW	12 mA	O	
F11	D15	A19						
D15	C16	A20						
C16	C15	A21						
B16	C14	A22						
A15	B15	A23						
A13	E11	A24						
G8	D8	A25/SCIO	• Async Memory Address Bus • Smart Card Interface I/O (Data)	LOW: A25	LOW	12 mA	I/O	
F8	B7	A26/SCCLK	• Async Memory Address Bus • Smart Card Interface Clock	LOW: A26	LOW	12 mA	I/O	
A8	A7	A27/SCRST	• Async Memory Address Bus • Smart Card Interface Reset	LOW: A27	LOW	12 mA	O	
D8	C8	nOE	Async Memory Output Enable	HIGH	No Change	12 mA	O	
C8	F8	nWE0	Async Memory Write Byte Enable 0	HIGH	No Change	12 mA	O	
D10	D9	nWE3	Async Memory Write Byte Enable 3	HIGH	No Change	8 mA	O	
B10	E9	CS6/SCKE1_2	• Async Memory Chip Select 6 • Sync Memory Clock Enable 1 or 2	LOW: CS6	No Change	12 mA	O	
C10	A10	CS7/SCKE0	• Async Memory Chip Select 7 • Sync Memory Clock Enable 0	LOW: CS7	No Change	12 mA	O	
G9	A11	SCKE3	Sync Memory Clock Enable 3	LOW	LOW	12 mA	O	
A10	B10	SCLK	Sync Memory Clock	LOW	No Change		I/O	2
C14	C13	nSCS0	Sync Memory Chip Select 0	HIGH	No Change	12 mA	O	

Table 3. Functional Pin List (Cont'd)

BGA PIN	LFBGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
D13	A15	nSCS1	Sync Memory Chip Select 1	HIGH	No Change	12 mA	O	
E11	D11	nSCS2	Sync Memory Chip Select 2	HIGH	No Change	12 mA	O	
A12	E10	nSCS3	Sync Memory Chip Select 3	HIGH	No Change	12 mA	O	
C12	A13	nSWE	Sync Memory Write Enable	HIGH	No Change	12 mA	O	
C11	B11	nCAS	Sync Memory Column Address Strobe Signal	HIGH	No Change	12 mA	O	
F9	C11	nRAS	Sync Memory Row Address Strobe Signal	HIGH	No Change	12 mA	O	
A9	C9	DQM0	Sync Memory Data Mask 0	HIGH	No Change	12 mA	O	
B9	A9	DQM1	Sync Memory Data Mask 1	HIGH	No Change	12 mA	O	
D9	B9	DQM2	Sync Memory Data Mask 2	HIGH	No Change	12 mA	O	
E9	A8	DQM3	Sync Memory Data Mask 3	HIGH	No Change	12 mA	O	
J5	K1	PA0/LCDVD16	• GPIO Port A • LCD Data bit 16. This CLCDC output signal is always LOW.	Input: PA0	No Change	8 mA	I/O	
K1	K2	PA1/LCDVD17	• GPIO Port A • LCD Data bit 17. This CLCDC output signal is always LOW.	Input: PA1	No Change	8 mA	I/O	
K2	K3	PA2	GPIO Port A	Input	No Change	8 mA	I/O	
K3	K4	PA3					I/O	
K5	K6	PA4					I/O	
L1	K5	PA5					I/O	
L2	L1	PA6					I/O	
L3	L2	PA7					I/O	
L4	L3	PB0/ UARTRX1	• GPIO Port B • UART1 Receive Data Input	Input: PB0	No Change	8 mA	I/O	
L5	M1	PB1/UARTTX3	• GPIO Port B • UART3 Transmit Data Out	Input: PB1	LOW if PINMUX: UART3CON = 1 (bit 3); otherwise No Change	8 mA	I/O	
L7	M2	PB2/ UARTRX3	• GPIO Port B • UART3 Receive Data In	Input: PB2	No Change	8 mA	I/O	
M2	M3	PB3/ UARTCTS3	• GPIO Port B • UART3 Clear to Send	Input: PB3	No Change	8 mA	I/O	
M4	L5	PB4/ UARTDCD3	• GPIO Port B • UART3 Data Carrier Detect	Input: PB4	No Change	8 mA	I/O	
N1	N1	PB5/ UARTDSR3	• GPIO Port B • UART3 Data Set Ready	Input: PB5	No Change	8 mA	I/O	
N2	N2	PB6/SWID/ SMBD	• GPIO Port B • Single Wire Data • Smart Battery Data	Input: PB6	No Change	8 mA	I/O	
N3	M4	PB7/ SMBCLK	• GPIO Port B • Smart Battery Clock	Input: PB7	No Change	8 mA	I/O	7
P1	P1	PC0/ UARTTX1	• GPIO Port C • UART1 Transmit Data Output	LOW: PC0	No Change	12 mA	I/O	
P2	P2	PC1/LCDPS	• GPIO Port C • HR-TFT Power Save	LOW: PC1	No Change	12 mA	I/O	
R1	R1	PC2/ LCDVDDEN	• GPIO Port C • HR-TFT Power Sequence Control	LOW: PC2	No Change	12 mA	I/O	
K6	M5	PC3/LCDREV	• GPIO Port C • HR-TFT Gray Scale Voltage Reverse	LOW: PC3	No Change	12 mA	I/O	
L8	P3	PC4/ LCDSPS	• GPIO Port C • HR-TFT Reset Row Driver Counter	LOW: PC4	No Change	12 mA	I/O	

Table 3. Functional Pin List (Cont'd)

BGA PIN	LFBGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
T1	N4	PC5/ LCDCLS	• GPIO Port C • HR-TFT Row Driver Clock	LOW: PC5	No Change	12 mA	I/O	
T2	R2	PC6/LCDHR-LP	• GPIO Port C • LCD Latch Pulse	LOW: PC6	No Change	12 mA	I/O	
R2	N5	PC7/ LCDSPL	• GPIO Port C • LCD Start Pulse Left	LOW: PC7	No Change	12 mA	I/O	
M11	M9	PD0/LCDVD8	• GPIO Port D • LCD Video Data Bus	LOW: PD0	LOW if PINMUX: PDOCON = 1 (bit 1); otherwise, No Change	12 mA	I/O	
L11	K10	PD1/LCDVD9		LOW: PD1			I/O	
K8	P10	PD2/LCDVD10		LOW: PD2			I/O	
N11	T11	PD3/LCDVD11		LOW: PD3			I/O	
R9	T12	PD4/LCDVD12		LOW: PD4			I/O	
T9	R11	PD5/LCDVD13		LOW: PD5			I/O	
P10	R12	PD6/LCDVD14		LOW: PD6			I/O	
R10	T13	PD7/LCDVD15		LOW: PD7			I/O	
L10	T9	PE0/LCDVD4	• GPIO Port E • LCD Video Data Bus	Input: PE0	LOW if PINMUX: PDOCON or PEOCON = 1 (bits [1:0]); otherwise No Change	12 mA	I/O	
N10	K9	PE1/LCDVD5		Input: PE1			I/O	
M9	T10	PE2/LCDVD6		Input: PE2			I/O	
M10	R10	PE3/LCDVD7		Input: PE3			I/O	
A6	A5	PF0/INT0	• GPIO Port F • External FIQ Interrupt. Interrupts can be level or edge triggered and are internally debounced.	Input: PF0	No Change	8 mA	I/O	3
B6	B4	PF1/INT1	• GPIO Port F • External IRQ Interrupts. Interrupts can be level or edge triggered and are internally debounced.	Input: PF1	No Change	8 mA	I/O	3
C6	E7	PF2/INT2		Input: PF2	No Change	8 mA	I/O	3
H8	B3	PF3/INT3	• GPIO Port F • External IRQ Interrupt. Interrupts can be level or edge triggered and are internally debounced.	Input: PF3	No Change	8 mA	I/O	3
B5	C5	PF4/INT4/ SCVCCEN	• GPIO Port F • External IRQ Interrupt. Interrupts can be level or edge triggered and are internally debounced. • Smart Card Supply Voltage Enable	Input: PF4	LOW if SCI is Enabled; otherwise No Change	8 mA	I/O	3
D6	D6	PF5/INT5/ SCDETECT	• GPIO Port F • External IRQ Interrupt. Interrupts can be level or edge triggered and are internally debounced. • Smart Card Detection	Input: PF5	No Change	8 mA	I/O	3
E6	A4	PF6/INT6/ PCRDY1	• GPIO Port F • External IRQ Interrupt. Interrupts can be level or edge triggered and are internally debounced. • Ready for Card 1 for PC Card (PCMCIA or CF) in single or dual card mode	Input: PF6	No Change	8 mA	I/O	3
C5	A3	PF7/INT7/ PCRDY2	• GPIO Port F • External IRQ Interrupt. Interrupts can be level or edge triggered and are internally debounced. • Ready for Card 2 for PC Card (PCMCIA or CF) in single or dual card mode	Input: PF7	No Change	8 mA	I/O	3
R3	M6	PG0/nPCOE	• GPIO Port G • Output Enable for PC Card (PCMCIA or CF) in single or dual card mode	LOW: PG0	No Change	8 mA	I/O	
T3	T1	PG1/nPCWE	• GPIO Port G • Write Enable for PC Card (PCMCIA or CF) in single or dual card mode	LOW: PG1	No Change	8 mA	I/O	

Table 3. Functional Pin List (Cont'd)

BGA PIN	LFBGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
L6	P4	PG2/ nPCIOR	• GPIO Port G • I/O Read Strobe for PC Card (PCMCIA or CF) in single or dual card mode	LOW: PG2	No Change	8 mA	I/O	
M6	R3	PG3/ nPCIOW	• GPIO Port G • I/O Write Strobe for PC Card (PCMCIA or CF) in single or dual card mode	LOW: PG3	No Change	8 mA	I/O	
N6	T2	PG4/nPCREG	• GPIO Port G • Register Memory Access for PC Card (PCMCIA or CF) in single or dual card mode	LOW: PG4	No Change	8 mA	I/O	
M7	P5	PG5/nPCCE1	• GPIO Port G • Card Enable 1 for PC Card (PCMCIA or CF) in single or dual card mode. This signal and nPCCE2 are used by the PC Card for decoding low and high byte accesses.	LOW: PG5	No Change	8 mA	I/O	
M8	R4	PG6/nPCCE2	• GPIO Port G • Card Enable 2 for PC Card (PCMCIA or CF) in single or dual card mode. This signal and nPCCE1 are used by the PC Card for decoding low and high byte accesses.	LOW: PG6	No Change	8 mA	I/O	
N4	T3	PG7/PCDIR	• GPIO Port G • Direction for PC Card (PCMCIA or CF) in single or dual card mode	LOW: PG7	No Change	8 mA	I/O	
P4	P6	PH0/ PCRESET1	• GPIO Port H • Reset Card 1 for PC Card (PCMCIA or CF) in single or dual card mode	Input: PH0	No Change	8 mA	I/O	
R4	T4	PH1/CFA8/ PCRESET2	• GPIO Port H • Address Bit 8 for PC Card (CF) in single card mode • Reset Card 2 for PC Card (PCMCIA or CF) in dual card mode	Input: PH1	No Change	8 mA	I/O	
T4	M7	PH2/ nPCSLOTE1	• GPIO Port H • Enable Card 1 for PC Card (PCMCIA or CF) in single or dual card mode. This signal is used for gating other control signals to the appropriate PC Card.	Input: PH2	No Change	8 mA	I/O	
N7	T5	PH3/CFA9/ PCMCIAA25/ nPCSLOTE2	• GPIO Port H • Address Bit 9 for PC Card (CF) in single card mode • Address Bit 25 for PC Card (PCMCIA) in single card mode • Enable Card 2 for PC Card (PCMCIA or CF) in dual card mode. This signal is used for gating other control signals to the appropriate PC Card.	Input: PH3	No Change	8 mA	I/O	
P8	R6	PH4/ nPCWAIT1	• GPIO Port H • WAIT Signal for Card 1 for PC Card (PCMCIA or CF) in single or dual card mode	Input: PH4	No Change	8 mA	I/O	
P5	R7	PH5/CFA10/ PCMCIAA24/ nPCWAIT2	• GPIO Port H • Address Bit 10 for PC Card (CF) in single card mode • Address Bit 24 for PC Card (PCMCIA) in single card mode • WAIT Signal for Card 2 for PC Card (PCMCIA or F) in dual card mode	Input: PH5	No Change	8 mA	I/O	
R5	P7	PH6/ nAC97RESET	• GPIO Port H • Audio Codec (AC97) Reset	Input: PH6	No Change	8 mA	I/O	
T5	T6	PH7/ nPCSTATRE	• GPIO Port H • Status Read Enable for PC Card (PCMCIA or F) in single or dual card mode	Input: PH7	No Change	8 mA	I/O	
R6	T7	LCDFP	LCD Frame Synchronization pulse	LOW	LOW	12 mA	O	
R8	R9	LCDLP	LCD Line Synchronization pulse	LOW	LOW	12 mA	O	

Table 3. Functional Pin List (Cont'd)

BGA PIN	LFBGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
P9	P9	LCDENAB/ LCDM	LCD TFT Data Enable LCD STN AC Bias	LOW: LCDENAB	LOW	12 mA	O	
N9	N9	LCDDCLK	LCD Data Clock	LOW	LOW	12 mA	O	
P7	M8	LCDVD0	LCD Video Data Bus	LOW	LOW	12 mA	O	
R7	P8	LCDVD1					O	
T7	R8	LCDVD2					O	
N8	T8	LCDVD3					O	
T15	T16	USBDP	USB Data Positive (Differential Pair)	Input	No Change		I/O	10
T16	R16	USBDN	USB Data Negative (Differential Pair)	Input	No Change		I/O	10
E7	C7	nPWME0	• DC-DC Converter Pulse Width • Modulator 0 Enable	Input	No Change		I	
D7	A6	nPWME1	• DC-DC Converter Pulse Width • Modulator 1 Enable	Input	No Change		I	
C7	B6	PWM0	• DC-DC Converter Pulse Width • Modulator 0 Output during normal operation and Polarity Selection input at reset	Input	No Change	8 mA	I/O	
B7	B5	PWM1	• DC-DC Converter Pulse Width • Modulator 1 Output during normal operation and Polarity Selection input at reset	Input	No Change	8 mA	I/O	
C4	A2	ACBITCLK	• Audio Codec (AC97) Clock • Audio Codec (ACI) Clock	Input	No Change	8 mA	I/O	
D5	A1	ACOUT	• Audio Codec (AC97) Output • Audio Codec (ACI) Output	LOW	No Change	8 mA	O	
B4	B2	ACSYNC	• Audio Codec (AC97) Synchronization • Audio Codec (ACI) Synchronization	LOW	No Change	8 mA	O	
A4	E6	ACIN	• Audio Codec (AC97) Input • Audio Codec (ACI) Input	Input	No Change		I	
A3	C3	MMCCLK/ MMSPICLK	• MultiMediaCard Clock (20 MHz MAX.) • MultiMediaCard SPI Mode Clock	LOW: MMCCLK	LOW	8 mA	O	
B3	B1	MMCCMD/ MMSPIDIN	• MultiMediaCard Command • MultiMediaCard SPI Mode Data Input	Input: MMCCMD	Input	8 mA	I/O	
A2	D4	MMCDATA/ MMSPIDOUT	• MultiMediaCard Data • MultiMediaCard SPI Mode Data Output	Input: MMCDATA	Input	8 mA	I/O	
E2	E1	UARTCTS2	• UART2 Clear to Send Signal. This pin is an output for JTAG boundary scan only.	Input	No Change		I	
E3	F3	UARTDCD2	• UART2 Data Carrier Detect Signal. This pin is output for JTAG boundary scan only.	Input	No Change		I	
E5	G4	UARTDSR2	UART2 Data Set Ready Signal	Input	No Change		I	
F2	G5	UARTIRTX1	IrDA Transmit	LOW	No Change	8 mA	O	
F3	G6	UARTIRRX1	IrDA Receive. This pin is an output for JTAG boundary scan only.	Input	No Change		I	
F4	F1	UARTTX2	UART2 Transmit Data Output	HIGH	No Change	8 mA	O	
J7	G3	UARTRX2	UART2 Receive Data Input. This pin is an output for JTAG boundary scan only.	Input	No Change		I	
H4	J3	SSPCLK	Synchronous Serial Port Clock	LOW	No Change	8 mA	O	
J1	J6	SSPRX	Synchronous Serial Port Receive	Input	No Change		I	
J2	J7	SSPTX	Synchronous Serial Port Transmit	LOW	LOW	8 mA	I/O	
J3	J2	SSPFRM/ nSSPFRM	Synchronous Serial Port Frame Sync	Input	Input	8 mA	I/O	

Table 3. Functional Pin List (Cont'd)

BGA PIN	LFBGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
F6	G2	COL0	Keyboard Interface	HIGH	HIGH	8 mA	O	
F5	G1	COL1						
G1	H3	COL2						
G2	H5	COL3						
G4	H6	COL4						
G5	H7	COL5						
H1	H2	COL6						
H2	H1	COL7						
H3	J1	TBUZ	Timer Buzzer (254 kHz MAX.)	LOW	LOW	8 mA	O	
C3	F5	MEDCHG	Boot Device Media Change. Used with WIDTH0 and WIDTH1 to specify boot memory device.	Input	No Change		I	3
P11	T14	WIDTH0	External Memory Width Pins. Also, used with MEDCHG to specify the boot memory device size. The pins must be pulled HIGH with a 33 kΩ resistor.	Input	No Change		I	3
R12	T15	WIDTH1						
D1	E3	BATOK	Battery OK	Input	No Change		I	3
D2	F6	nBATCHG	Battery Change	Input	No Change		I	3
A1	E5	TDI	JTAG Data In. This signal is internally pulled-up t o VDD.	Input	No Change		I	4
B1	C2	TCK	JTAG Clock. This signal should be externally pulled-up to VDD with a 33 kΩ resistor.	Input	No Change		I	3
B2	D3	TDO	JTAG Data Out. This signal should be externally pulled up to VDD with a 33 kΩ resistor.	High-Z	No Change	4 mA	O	
C1	C1	TMS	JTAG Test Mode select. This signal is internally pulled-up to VDD.	Input	No Change		I	4
T12	P15	nTEST0	Test Pin 0. Internally pulled up to VDD. For Normal mode, leave open. For JTAG mode, tie to GND. See Table 4.	Input	No Change		I	4
R15	P13	nTEST1	Test Pin 1. internally pulled up to VDD. For Normal and JTAG mode, leave open. See Table 4.					

1. Signals beginning with 'n' are Active LOW.
2. The SCLK pin can source up to 12 mA and sink up to 20 mA. See 'DC Characteristics'.
3. Schmitt trigger input; see 'DC Specifications', page 31 for triggers points and hysteresis.
4. Input only for JTAG boundary scan mode.
5. Output only for JTAG boundary scan mode.
6. The internal pullup and pull-down resistance on all digital I/O pins is 50 kΩ
7. When used as SMBCLK, this pin must have a resistor.
8. The RESET STATE is defined as the state during power-on reset.
9. The STANDBY STATE is defined as the state when the device is in standby. During this state, I/O cells are forced to input (Input), output driving low (LOW), output driving high (HIGH), or their current state is preserved (No Change). In some case, function selection has an overall effect on the standby state.
10. All unused USB Device pins with a differential pair must be pulled to ground with a 15 kΩ resistor.

Table 4. nTest Pin Function

MODE	nTEST0	nTEST1	nURESET
JTAG	0	1	1
Normal	1	1	x

Table 5. LCD Data Multiplexing

BGA PIN	LFBGA PIN	LCD DATA SIGNAL	STN						TFT	AD-TFT/ HR-TFT
			MONO 4-BIT		MONO 8-BIT		COLOR			
			SINGLE PANEL	DUAL PANEL	SINGLE PANEL	DUAL PANEL	SINGLE PANEL	DUAL PANEL		
K1	K2	LCDVD17								LOW
J5	K1	LCDVD16								LOW
R10	T13	LCDVD15				MLSTN7		CLSTN7	Intensity	Intensity
P10	R12	LCDVD14				MLSTN6		CLSTN6	BLUE4	BLUE4
T9	R11	LCDVD13				MLSTN5		CLSTN5	BLUE3	BLUE3
R9	T12	LCDVD12				MLSTN4		CLSTN4	BLUE2	BLUE2
N11	T11	LCDVD11				MLSTN3		CLSTN3	BLUE1	BLUE1
K8	P10	LCDVD10				MLSTN2		CLSTN2	BLUE0	BLUE0
L11	K10	LCDVD9				MLSTN1		CLSTN1	GREEN4	GREEN4
M11	M9	LCDVD8				MLSTN0		CLSTN0	GREEN3	GREEN3
M10	R10	LCDVD7		MLSTN3	MUSTN7	MUSTN7	CUSTN7	CUSTN7	GREEN2	GREEN2
M9	T10	LCDVD6		MLSTN2	MUSTN6	MUSTN6	CUSTN6	CUSTN6	GREEN1	GREEN1
N10	K9	LCDVD5		MLSTN1	MUSTN5	MUSTN5	CUSTN5	CUSTN5	GREEN0	GREEN0
L10	T9	LCDVD4		MLSTN0	MUSTN4	MUSTN4	CUSTN4	CUSTN4	RED4	RED4
N8	T8	LCDVD3	MUSTN3	MUSTN3	MUSTN3	MUSTN3	CUSTN3	CUSTN3	RED3	RED3
T7	R8	LCDVD2	MUSTN2	MUSTN2	MUSTN2	MUSTN2	CUSTN2	CUSTN2	RED2	RED2
R7	P8	LCDVD1	MUSTN1	MUSTN1	MUSTN1	MUSTN1	CUSTN1	CUSTN1	RED1	RED1
P7	M8	LCDVD0	MUSTN0	MUSTN0	MUSTN0	MUSTN0	CUSTN0	CUSTN0	RED0	RED0

Notes:
1. The Intensity bit is identically generated for all three colors.
2. MU = Monochrome Upper
3. CU = Color Upper
4. CL = Color Lower

Table 6. 256-Ball BGA Package Numerical Pin List

BGA PIN	SIGNAL
A1	TDI
A2	MMCDATA/MMSPIDOUT
A3	MMCCLK/MMSPICLK
A4	ACIN
A5	VSS
A6	PF0/INT0
A7	VDDC
A8	A27/SCRST
A9	DQM0
A10	SCLK
A11	VSS
A12	nSCS3
A13	A24
A14	D24
A15	A23
A16	D23
B1	TCK
B2	TDO
B3	MMCCMD/MMSPIDIN
B4	ACSYNC
B5	PF4/INT4/SCVCCEN
B6	PF1/INT1
B7	PWM1
B8	VDD
B9	DQM1
B10	CS6/SCKE1_2
B11	D30
B12	D29
B13	D25
B14	VDD
B15	VSSC
B16	A22
C1	TMS
C2	nEXTPWR
C3	MEDCHG
C4	ACBITCLK
C5	PF7/INT7/PCRDY2
C6	PF2/INT2
C7	PWM0
C8	nWE0
C9	VSSC
C10	CS7/SCKE0
C11	nCAS
C12	nSWE
C13	D26

Table 6. 256-Ball BGA Package Numerical Pin List (Cont'd)

BGA PIN	SIGNAL
C14	nSCS0
C15	VSS
C16	A21
D1	BATOK
D2	nBATCHG
D3	nPOR
D4	WAKEUP
D5	ACOUT
D6	PF5/INT5/SCDETECT
D7	nPWME1
D8	nOE
D9	DQM2
D10	nWE3
D11	D31
D12	VDDC
D13	nSCS1
D14	D21
D15	A20
D16	D19
E1	VDDC
E2	UARTCTS2
E3	UARTDCD2
E4	nPWRFL
E5	UARTDSR2
E6	PF6/INT6/PCRDY1
E7	nPWME0
E8	VSS
E9	DQM3
E10	VDD
E11	nSCS2
E12	D27
E13	A18
E14	D18
E15	VDDC
E16	A17/SB1
F1	VDD
F2	UARTIRTX1
F3	UARTIRRX1
F4	UARTTX2
F5	COL1
F6	COL0
F7	VSS
F8	A26/SCCLK
F9	nRAS
F10	D22

Table 6. 256-Ball BGA Package Numerical Pin List (Cont'd)

BGA PIN	SIGNAL
F11	A19
F12	D17
F13	VDD
F14	A16/SB0
F15	D16
F16	A15/SA13
G1	COL2
G2	COL3
G3	VSS
G4	COL4
G5	COL5
G6	VSSC
G7	VDD
G8	A25/SCIO
G9	SCKE3
G10	D28
G11	D14
G12	D15
G13	A14/SA12
G14	A13/SA11
G15	D13
G16	A12/SA10
H1	COL6
H2	COL7
H3	TBUZ
H4	SSPCLK
H5	VSSC
H6	nURESET
H7	VSS
H8	PF3/INT3
H9	VSS
H10	D20
H11	D6
H12	VSSC
H13	D12
H14	A11/SA9
H15	D11
H16	A10/SA8
J1	SSPRX
J2	SSPTX
J3	SSPFRM/nSSPFRM
J4	VDDC
J5	PA0/LCDVD16
J6	PGMCLK
J7	UARTRX2

Table 6. 256-Ball BGA Package Numerical Pin List (Cont'd)

BGA PIN	SIGNAL
J8	A6/SA4
J9	A9/SA7
J10	D10
J11	VDD
J12	VDD
J13	D9
J14	A8/SA6
J15	D8
J16	A7/SA5
K1	PA1/LCDVD17
K2	PA2
K3	PA3
K4	VSS
K5	PA4
K6	PC3/LCDREV
K7	VDD
K8	PD2/LCDVD10
K9	VDDC
K10	nCS1
K11	nCS0
K12	D7
K13	VSS
K14	A5/SA3
K15	A4/SA2
K16	A3/SA1
L1	PA5
L2	PA6
L3	PA7
L4	PB0/UARTRX1
L5	PB1/UARTTX3
L6	PG2/nPCIOR
L7	PB2/UARTRX3
L8	PC4/LCDSPS
L9	VSSC
L10	PE0/LCDVD4
L11	PD1/LCDVD9
L12	D0
L13	VDDC
L14	D5
L15	D4
L16	D3
M1	VDD
M2	PB3/UARTCTS3
M3	VSSC

Table 6. 256-Ball BGA Package Numerical Pin List (Cont'd)

BGA PIN	SIGNAL
M4	PB4/UARTDCD3
M5	VDD
M6	PG3/nPCIOW
M7	PG5/nPCCE1
M8	PG6/nPCCE2
M9	PE2/LCDVD6
M10	PE3/LCDVD7
M11	PD0/LCDVD8
M12	nCS3/nMMSPICS
M13	A2/SA0
M14	VDD
M15	D1
M16	A0/nWE1
N1	PB5/UARTDSR3
N2	PB6/SWID/SMBD
N3	PB7/SMBCLK
N4	PG7/PCDIR
N5	VSS
N6	PG4/nPCREG
N7	PH3/CFA9/PCMCIAA25/nPCSLOTE2
N8	LCDVD3
N9	LCDDCLK
N10	PE1/LCDVD5
N11	PD3/LCDVD11
N12	VDDA
N13	D2
N14	A1/nWE2
N15	VSSC
N16	VSS
P1	PC0/UARTTX1
P2	PC1/LCDPS
P3	VDDC
P4	PH0/PCRESET1
P5	PH5/CFA10/PCMCIAA24/nPCWAIT2
P6	VSS
P7	LCDVD0
P8	PH4/nPCWAIT1
P9	LCDENAB/LCDM
P10	PD6/LCDVD14
P11	WIDTH0
P12	VSSA
P13	nCS2
P14	CLKEN
P15	XTAL32OUT

Table 6. 256-Ball BGA Package Numerical Pin List (Cont'd)

BGA PIN	SIGNAL
P16	XTAL32IN
R1	PC2/LCDVDDEN
R2	PC7/LCDSPL
R3	PG0/nPCOE
R4	PH1/CFA8/PCRESET2
R5	PH6/nAC97RESET
R6	LCDFP
R7	LCDVD1
R8	LCDLP
R9	PD4/LCDVD12
R10	PD7/LCDVD15
R11	VDDA
R12	WIDTH1
R13	XTALIN
R14	VDD
R15	nTEST1
R16	VSS
T1	PC5/LCDCLS
T2	PC6/LCDHRLP
T3	PG1/nPCWE
T4	PH2/nPCSLOTE1
T5	PH7/nPCSTATRE
T6	VDD
T7	LCDVD2
T8	VDDC
T9	PD5/LCDVD13
T10	VSSC
T11	VSSA
T12	nTEST0
T13	XTALOUT
T14	VSS
T15	USBDP
T16	USBDN

Table 7. 256-Ball LFBGA Package Numerical Pin List

LFBGA PIN	SIGNAL
A1	ACOUT
A2	ACBITCLK
A3	PF7/INT7/PCRDY2
A4	PF6/INT6/PCRDY1
A5	PF0/INT0
A6	nPWME1
A7	A27/SCRST
A8	DQM3
A9	DQM1
A10	CS7/SCKE0
A11	SCKE3
A12	D31
A13	nSWE
A14	D29
A15	nSCS1
A16	D25
B1	MMCCMD/MMSPIDIN
B2	ACSYNC
B3	PF3/INT3
B4	PF1/INT1
B5	PWM1
B6	PWM0
B7	A26/SCCLK
B8	VSS
B9	DQM2
B10	SCLK
B11	nCAS
B12	D30
B13	D26
B14	D27
B15	A23
B16	D23
C1	TMS
C2	TCK
C3	MMCCLK/MMSPICLK
C4	VDDC
C5	PF4/INT4/SCVCCEN
C6	VSS
C7	nPWME0
C8	nOE
C9	DQM0
C10	VDD
C11	nRAS
C12	D28
C13	nSCS0

Table 7. 256-Ball LFBGA Package Numerical Pin List

LFBGA PIN	SIGNAL
C14	A22
C15	A21
C16	A20
D1	nURESET
D2	nEXTPWR
D3	TDO
D4	MMCDATA/MMSPIDOUT
D5	VSS
D6	PF5/INT5/SCDETECT
D7	VDDC
D8	A25/SCIO
D9	nWE3
D10	VDDC
D11	nSCS2
D12	D24
D13	VSS
D14	D21
D15	A19
D16	D18
E1	UARTCTS2
E2	WAKEUP
E3	BATOK
E4	nPOR
E5	TDI
E6	ACIN
E7	PF2/INT2
E8	VSS
E9	CS6/SCKE1_2
E10	nSCS3
E11	A24
E12	D22
E13	D20
E14	A18
E15	D17
E16	A16/SB0
F1	UARTTX2
F2	nPWRFL
F3	UARTDCD2
F4	VDDC
F5	MEDCHG
F6	nBATCHG
F7	VSS
F8	nWE0
F9	VDD

Table 7. 256-Ball LFBGA Package Numerical Pin List

LFBGA PIN	SIGNAL
F10	VDDC
F11	VDD
F12	D19
F13	A17/SB1
F14	VDD
F15	D16
F16	A15/SA13
G1	COL1
G2	COL0
G3	UARTRX2
G4	UARTDSR2
G5	UARTIRTX1
G6	UARTIRRX1
G7	VSSC
G8	VDD
G9	D13
G10	A13/SA11
G11	A14/SA12
G12	D15
G13	VSS
G14	D14
G15	A12/SA10
G16	D12
H1	COL7
H2	COL6
H3	COL2
H4	VSSC
H5	COL3
H6	COL4
H7	COL5
H8	VSSC
H9	VSS
H10	A10/SA8
H11	D11
H12	A11/SA9
H13	VDD
H14	D10
H15	A9/SA7
H16	D9
J1	TBUZ
J2	SSPFRM/nSSPFRM
J3	SSPCLK
J4	VDDC
J5	PGMCLK

Table 7. 256-Ball LFBGA Package Numerical Pin List

LFBGA PIN	SIGNAL
J6	SSPRX
J7	SSPTX
J8	VDDC
J9	VDD
J10	D8
J11	A7/SA5
J12	D7
J13	A6/SA4
J14	VSS
J15	D6
J16	A8/SA6
K1	PA0/LCDVD16
K2	PA1/LCDVD17
K3	PA2
K4	PA3
K5	PA5
K6	PA4
K7	VSS
K8	VDDC
K9	PE1/LCDVD5
K10	PD1/LCDVD9
K11	D3
K12	A3/SA1
K13	A4/SA2
K14	D5
K15	VDD
K16	A5/SA3
L1	PA6
L2	PA7
L3	PB0/UARTRX1
L4	VSSC
L5	PB4/UARTDCD3
L6	VDDC
L7	VDD
L8	VSS
L9	VSSC
L10	VSS
L11	D0
L12	VSS
L13	D1
L14	D2
L15	A2/SA0
L16	D4
M1	PB1/UARTTX3

Table 7. 256-Ball LFBGA Package Numerical Pin List

LFBGA PIN	SIGNAL
M2	PB2/UARTRX3
M3	PB3/UARTCTS3
M4	PB7/SMBCLK
M5	PC3/LCDREV
M6	PG0/nPCOE
M7	PH2/nPCSLOTE1
M8	LCDVD0
M9	PD0/LCDVD8
M10	VDDA
M11	VSS
M12	CLKEN
M13	XTAL32OUT
M14	VSS
M15	A0/nWE1
M16	A1/nWE2
N1	PB5/UARTDSR3
N2	PB6/SWID/SMBD
N3	VSSC
N4	PC5/LCDCLS
N5	PC7/LCDSPL
N6	VDD
N7	VSSC
N8	VDD
N9	LCDDCLK
N10	VSSC
N11	VSSA
N12	VDD
N13	VDD
N14	XTAL32IN
N15	nCS2
N16	nCS3/nMMSPICS
P1	PC0/UARTTX1
P2	PC1/LCDPS
P3	PC4/LCDSPS
P4	PG2/nPCIOR
P5	PG5/nPCCE1
P6	PH0/PCRESET1
P7	PH6/AC97RESET
P8	LCDVD1
P9	LCDENAB/LCDM
P10	PD2/LCDVD10
P11	VDD
P12	VDDA
P13	nTEST1

Table 7. 256-Ball LFBGA Package Numerical Pin List

LFBGA PIN	SIGNAL
P14	nCS0
P15	nTEST0
P16	nCS1
R1	PC2/LCDVDDEN
R2	PC6/LCDHRLP
R3	PG3/nPCIOW
R4	PG6/nPCCE2
R5	VSSC
R6	PH4/nPCWAIT1
R7	PH5/CFA10/PCMCIAA24/nPCWAIT2
R8	LCDVD2
R9	LCDLP
R10	PE3/LCDVD7
R11	PD5/LCDVD13
R12	PD6/LCDVD14
R13	VSSA
R14	XTALIN
R15	XTALOUT
R16	USBDN
T1	PG1/nPCWE
T2	PG4/nPCREG
T3	PG7/PCDIR
T4	PH1/CFA8/PCRESET2
T5	PH3/CFA9/PCMCIAA25/nPCSLOTE2
T6	PH7/nPCSTATRE
T7	LCDFP
T8	LCDVD3
T9	PE0/LCDVD4
T10	PE2/LCDVD6
T11	PD3/LCDVD11
T12	PD4/LCDVD12
T13	PD7/LCDVD15
T14	WIDTH0
T15	WIDTH1
T16	USBDP

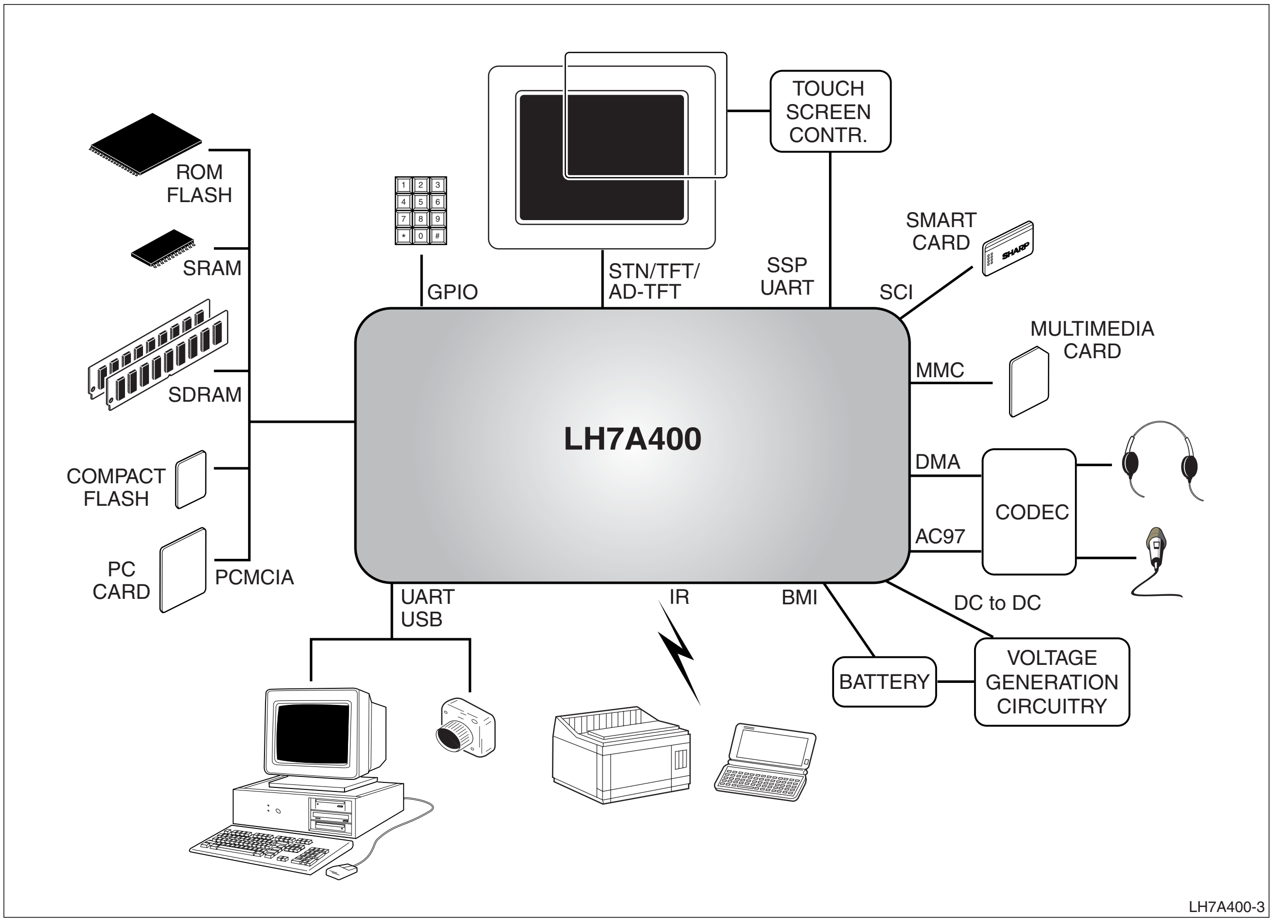


Figure 4. Application Diagram

SYSTEM DESCRIPTIONS

ARM922T Processor

The LH7A400 microcontroller features the ARM922T cached core with an Advanced High Performance Bus (AHB) interface. The processor is a member of the ARM9T family of processors. For more information, see the ARM document, 'ARM922T Technical Reference Manual', available on ARM's website at www.arm.com.

Clock and State Controller

The clocking scheme in the LH7A400 is based around two primary oscillator inputs. These are the 14.7456 MHz input crystal and the 32.768 kHz real time clock oscillator. See Figure 5. The 14.7456 MHz oscillator is used to generate the main system clock domains for the LH7A400, where as the 32.768 kHz is used for controlling the power down operations and real time clock peripheral. The clock and state controller provides the clock gating and frequency division necessary, and then supplies the clocks to the processor and to the rest of the system. The amount of clock gating that actually takes place is dependent on the current power saving mode selected.

The 32.768 kHz clock provides the source for the Real Time Clock tree and power-down logic.This clock is used for the power state control in the design and is the only clock in the LH7A400 that runs permanently. The 32.768 kHz clock is divided down to 1 Hz using a ripple divider to save power. This generated 1 Hz clock is used in the Real Time Clock counter.

The 14.7456 MHz source is used to generate the main system clocks for the LH7A400. It is the source for PLL1 and PLL2, it acts as the primary clock to the peripherals and is the source clock to the Programmable clock (PGM) divider.

PLL1 provides the main clock tree for the chip, it generates the following clocks: FCLK, HCLK and PCLK. FCLK is the clock that drives the ARM922T core. HCLK is the main bus (AHB) clock, as such it clocks all memory interfaces, bus arbitrators and the AHB peripherals. HCLK is generated by dividing FCLK by 1, 2, 3, or 4. HCLK can be gated by the system to enable low power operation. PCLK is the peripheral bus (APB) clock. It is generated by dividing HCLK by either 2, 4, or 8.

PLL2 is used to generate a fixed frequency of 48 MHz for the USB peripheral.

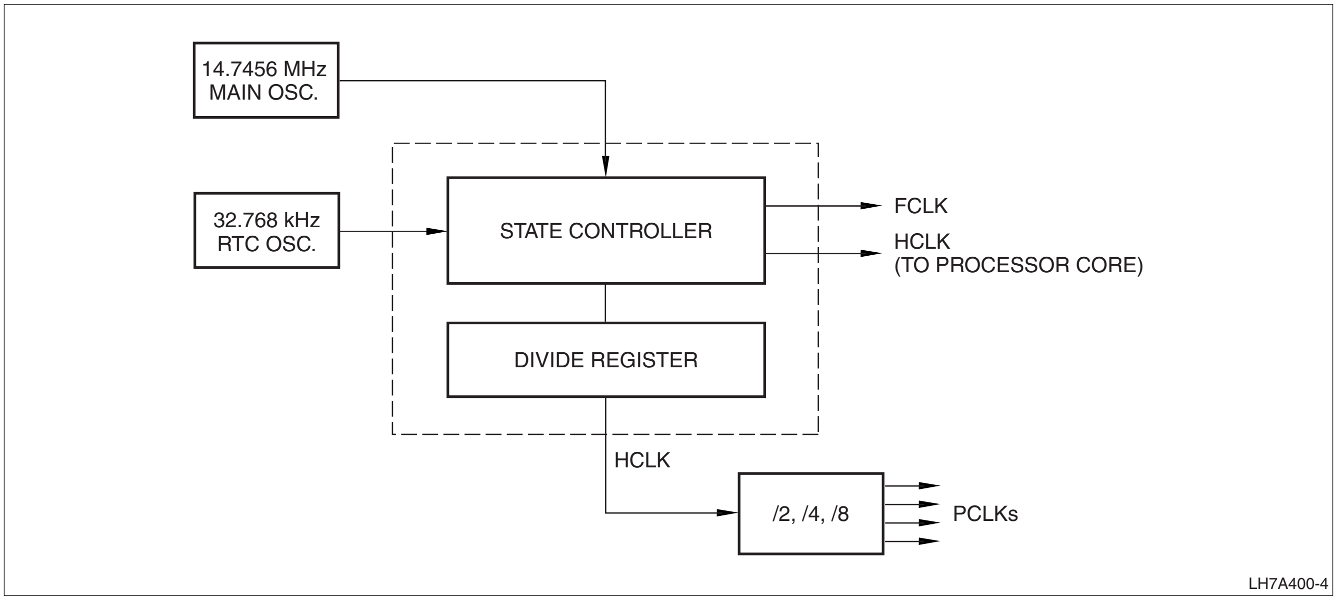


Figure 5. Clock and State Controller Block Diagram

Power Modes

The LH7A400 has three operational states: Run, Halt, and Standby. In Run mode, all clocks are hardware-enabled and the processor is clocked. Halt mode stops the processor clock while waiting for an event such as a key press, but the device continues to function. Finally, Standby equates to the computer being switched ‘off’, i.e. no display (LCD disabled) and the main oscillator is shut down. The 32.768 kHz oscillator operates in all three modes.

Reset Modes

There are three external signals that can generate resets to the LH7A400; these are nPOR (power on reset), nPWRFL (power failure) and nURESET (user reset). If any of these are active, a system reset is generated internally. A nPOR reset performs a full system reset. The nPWRFL and nURESET resets will perform a full system reset except for the SDRAM refresh control, SDRAM Global Configuration, SDRAM Device Configuration and the RTC peripheral registers. The SDRAM controller will issue a self-refresh command to external SDRAM before the system enters this reset (the nPWRFL and nURESET resets only, not so for the nPOR reset). This allows the system to maintain its Real Time Clock and SDRAM contents. On coming out of reset, the chip enters Standby mode. Once in Run mode the PWRSR register can be interrogated to determine the nature of the reset, and the trigger source, after which software can then take appropriate actions.

Data Paths

The data paths in the LH7A400 are:

- The AMBA AHB bus
- The AMBA APB bus
- The External Bus Interface
- The LCD AHB bus
- The DMA busses.

AMBA AHB BUS

The Advanced Microprocessor Bus Architecture Advanced High-performance Bus (AMBA AHB) bus is a high speed 32-bit-wide data bus. The AMBA AHB is for high-performance, high clock frequency system modules.

Peripherals that have high bandwidth requirements are connected to the LH7A400 core processor using the AHB bus. These include the external and internal memory interfaces, the LCD registers, palette RAM and the bridge to the Advanced Peripheral Bus (APB) interface. The APB Bridge transparently converts the AHB access into the slower speed APB accesses. All of the control registers for the APB peripherals are programmed using the AHB - APB bridge interface. The main AHB data and address lines are configured using a multiplexed bus. This removes the need for tri-state buffers and bus holders, and simplifies bus arbitration.

AMBA APB BUS

The AMBA APB bus is a lower-speed 32-bit-wide peripheral data bus. The speed of this bus is selectable to be a divide-by-2, divide-by-4 or divide-by-8 of the speed of the AHB bus.

EXTERNAL BUS INTERFACE

The External Bus Interface (EBI) provides a 32-bit wide, high speed gateway to external memory devices. The memory devices supported include:

- Asynchronous RAM/ROM/Flash
- Synchronous DRAM/Flash
- PCMCIA interfaces
- CompactFlash interfaces.

The EBI can be controlled by either the Asynchronous memory controller or Synchronous memory controller. There is an arbiter on the EBI input, with priority given to the Synchronous Memory Controller interface.

LCD AHB BUS

The LCD controller has its own local memory bus that connects it to the system's embedded memory and external SDRAM. The function of this local data bus is to allow the LCD controller to perform its video refresh function without congesting the AHB bus. This leads to better system performance and lower power consumption. There is an arbiter on both the embedded memory and the synchronous memory controller. In both cases the LCD bus is given priority.

DMA BUSES

The LH7A400 has a DMA system that connects the higher speed/higher data volume APB peripherals (MMC, USB and AC97) to the AHB bus. This enables the efficient transfer of data between these peripherals and external memory without the intervention of the ARM922T core. The DMA engine does not support memory to memory transfers.

Memory Map

The LH7A400 system has a 32-bit-wide address bus. This allows it to address up to 4GB of memory. This memory space is subdivided into a number of memory banks; see Figure 6. Four of these banks (each of 256MB) are allocated to the Synchronous memory controller. Eight of the banks (again, each 256MB) are allocated to the Asynchronous memory controller. Two of these eight banks are designed for PCMCIA systems. Part of the remaining memory space is allocated to the embedded SRAM, and to the control registers of the AHB and APB. The rest is unused.

The LH7A400 can boot from either synchronous or asynchronous ROM/Flash. The selection is determined by the value of the MEDCHG pin at Power On Reset as shown in Table 8. When booting from synchronous memory, then synchronous bank 4 (nSCS3) is mapped into memory location zero. When booting from asynchronous memory, asynchronous memory bank 0 (nSCS0) is mapped into memory location zero.

Figure 6 shows the memory map of the LH7A400 system for the two boot modes.

Once the LH7A400 has booted, the boot code can configure the ARM922T MMU to remap the low memory space to a location in RAM. This allows the user to set the interrupt vector table.

Table 8. Boot Modes

BOOT MODE	LATCHED BOOT-WIDTH1	LATCHED BOOT-WIDTH0	LATCHED MEDCHG
8-bit ROM	0	0	0
16-bit ROM	0	1	0
32-bit ROM	1	0	0
32-bit ROM	1	1	0
16-bit SFlash (Initializes Mode Register)	0	0	1
16-bit SROM (Initializes Mode Register)	0	1	1
32-bit SFlash (Initializes Mode Register)	1	0	1
32-bit SROM (Initializes Mode Register)	1	1	1

Interrupt Controller

The LH7A400 interrupt controller is designed to control the interrupts from 28 different sources. Four interrupt sources are mapped to the FIQ input of the ARM922T and 24 are mapped to the IRQ input. FIQs have a higher priority than the IRQs. If two interrupts with the same priority become active at the same time, the priority must be resolved in software.

When an interrupt becomes active, the interrupt controller generates an FIQ or IRQ if the corresponding mask bit is set. No latching of interrupts takes place in the controller. After a Power On Reset all mask register bits are cleared, therefore masking all interrupts. Hence, enabling of the mask register must be done by software after a power-on-reset.

Address	SYNCHRONOUS MEMORY BOOT	ASYNCHRONOUS MEMORY BOOT	Size
F000.0000	ASYNCHRONOUS MEMORY (nCS0)	SYNCHRONOUS MEMORY (nSCS3)	256MB
E000.0000	SYNCHRONOUS MEMORY (nSCS2)	SYNCHRONOUS MEMORY (nSCS2)	256MB
D000.0000	SYNCHRONOUS MEMORY (nSCS1)	SYNCHRONOUS MEMORY (nSCS1)	256MB
C000.0000	SYNCHRONOUS MEMORY (nSCS0)	SYNCHRONOUS MEMORY (nSCS0)	256MB
B001.4000	RESERVED	RESERVED	
B000.0000	EMBEDDED SRAM	EMBEDDED SRAM	80KB
8000.3800	RESERVED	RESERVED	
8000.2000	AHB INTERNAL REGISTERS	AHB INTERNAL REGISTERS	
8000.0000	APB INTERNAL REGISTERS	APB INTERNAL REGISTERS	
7000.0000	ASYNCHRONOUS MEMORY (CS7)	ASYNCHRONOUS MEMORY (CS7)	256MB
6000.0000	ASYNCHRONOUS MEMORY (CS6)	ASYNCHRONOUS MEMORY (CS6)	256MB
5000.0000	PCMCIA/CompactFlash (nPCSLOTE2)	PCMCIA/CompactFlash (nPCSLOTE2)	256MB
4000.0000	PCMCIA/CompactFlash (nPCSLOTE1)	PCMCIA/CompactFlash (nPCSLOTE1)	256MB
3000.0000	ASYNCHRONOUS MEMORY (nCS3)	ASYNCHRONOUS MEMORY (nCS3)	256MB
2000.0000	ASYNCHRONOUS MEMORY (nCS2)	ASYNCHRONOUS MEMORY (nCS2)	256MB
1000.0000	ASYNCHRONOUS MEMORY (nCS1)	ASYNCHRONOUS MEMORY (nCS1)	256MB
0000.0000	SYNCHRONOUS ROM (nSCS3)	ASYNCHRONOUS ROM (nCS0)	256MB

LH7A400-6

Figure 6. Memory Mapping for Each Boot Mode

External Bus Interface

The external bus interface allows the ARM922T, LCD controller and DMA engine access to an external memory system. The LCD controller has access to an internal frame buffer in embedded SRAM and an extension buffer in Synchronous Memory for large displays. The processor and DMA engine share the main system bus, providing access to all external memory devices and the embedded SRAM frame buffer.

An arbitration unit ensures that control over the External Bus Interface (EBI) is only granted when an existing access has been completed. See Figure 7.

Embedded SRAM

The amount of Embedded SRAM contained in the LH7A400 is 80 kB. This Embedded memory is designed to be used for storing code, data, or LCD frame data and to be contiguous with external SDRAM. The 80 kB is large enough to store a QVGA panel (320 × 240) at 8 bits per pixel, equivalent to 70 kB of information.

Containing the frame buffer on chip reduces the overall power consumed in any application that uses the LH7A400. Normally, the system has to perform external accesses to acquire this data. The LCD controller is designed to automatically use an overflow frame buffer in SDRAM if a larger screen size is required. This overflow buffer can be located on any 4 kB page boundary in SDRAM, allowing software to set the MMU (in the LCD controller) page tables such that the two memory areas appear contiguous. Byte, Half-Word and Word accesses are permissible.

Asynchronous Memory Controller

The Asynchronous memory controller is incorporated as part of the memory controller to provide an interface between the AMBA AHB system bus and external (off-chip) memory devices.

The Asynchronous Memory Controller provides support for up to eight independently configurable memory banks simultaneously. Each memory bank is capable of supporting:

- SRAM
- ROM
- Flash EPROM
- Burst ROM memory.

Each memory bank may use devices using either 8-, 16-, or 32-bit external memory data paths. The memory controller supports only little-endian operation.

The memory banks can be configured to support:

- Non-burst read and write accesses only to high-speed CMOS static RAM.
- Non-burst write accesses, nonburst read accesses and asynchronous page mode read accesses to fast-boot block flash memory.

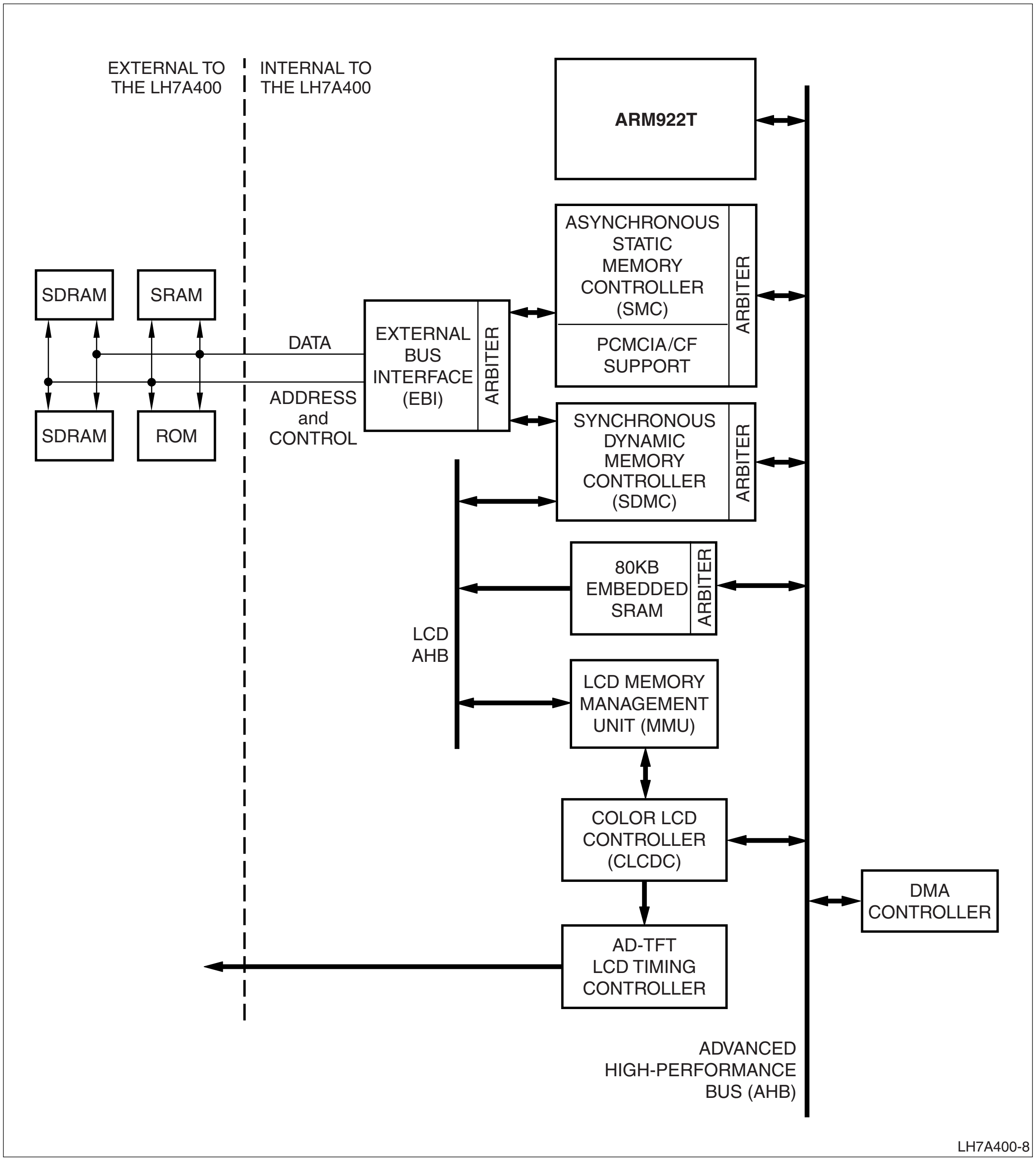


Figure 7. External Bus Interface Block Diagram

The Asynchronous Memory Controller has six main functions:

- Memory bank select
- Access sequencing
- Wait states generation
- Byte lane write control
- External bus interface
- CompactFlash or PCMCIA interfacing.

Synchronous Memory Controller

The Synchronous memory controller provides a high speed memory interface to a wide variety of Synchronous memory devices, including SDRAM, Synchronous Flash and Synchronous ROMs.

The key features of the controller are:

- LCD DMA port for high bandwidth
- Up to four Synchronous Memory banks that can be independently set up
- Special configuration bits for Synchronous ROM operation
- Ability to program Synchronous Flash devices using write and erase commands
- On booting from Synchronous ROM, (and optionally with Synchronous Flash), a configuration sequence is performed before releasing the processor from reset
- Data is transferred between the controller and the SDRAM in quad-word bursts. Longer transfers within the same page are concatenated, forming a seamless burst
- Programmable for 16- or 32-bit data bus size
- Two reset domains are provided to enable SDRAM contents to be preserved over a ‘soft’ reset
- Power saving Synchronous Memory SCKE and external clock modes provided.

MultiMediaCard (MMC)

The MMC adapter combines all of the requirements and functions of an MMC host. The adapter supports the full MMC bus protocol, defined by the MMC Definition Group’s specification v.2.11. The controller can also implement the SPI interface to the cards.

INTERFACE DESCRIPTION AND MMC OVERVIEW

The MMC controller uses the three-wire serial data bus (clock, command, and data) to transfer data to and from the MMC card, and to configure and acquire status information from the card’s registers.

MMC bus lines can be divided into three groups:

- Power supply: VDD and VSS
- Data Transfer: MMCCMD, MMCDATA
- Clock: MMCLK.

MULTIMEDIACARD ADAPTER

The MultiMediaCard Adapter implements MultiMediaCard specific functions, serves as the bus master for the MultiMediacard Bus and implements the standard interface to the MultiMediaCard Cards (card initialization, CRC generation and validation, command/response transactions, etc.).

Smart Card Interface (SCI)

The SCI (ISO7816) interfaces to an external Smart Card reader. The SCI can autonomously control data transfer to and from the smart card. Transmit and receive data FIFOs are provided to reduce the required interaction between the CPU core and the peripheral.

SCI FEATURES

- Supports asynchronous T0 and T1 transmission protocols
- Supports clock rate conversion factor F = 372, with bit rate adjustment factors D = 1, 2, or 4 supported
- Eight-character-deep buffered Tx and Rx paths
- Direct interrupts for Tx and Rx FIFO level monitoring
- Interrupt status register
- Hardware-initiated card deactivation sequence on detection of card removal
- Software-initiated card deactivation sequence on transaction complete
- Limited support for synchronous Smart Cards via registered input/output.

PROGRAMMABLE PARAMETERS

- Smart Card clock frequency
- Communication baud rate
- Protocol convention
- Card activation/deactivation time
- Check for maximum time for first character of Answer to Reset - ATR reception
- Check for maximum duration of ATR character stream
- Check for maximum time of receipt of first character of data stream
- Check for maximum time allowed between characters
- Character guard time
- Block guard time
- Transmit/receive character retry.

Direct Memory Access Controller (DMA)

The DMA Controller interfaces streams from the following three peripherals to the system memory:

- USB (1 Tx and 1 Rx DMA Channel)
- MMC (1 Tx and 1 Rx DMA Channel)
- AC97 (3 Tx and 3 Rx DMA Channels).

Each has its own bi-directional peripheral DMA bus capable of transferring data in both directions simultaneously. All memory transfers take place via the main system AHB bus.

DMA Specific features are:

- Independent DMA channels for Tx and Rx
- Two Buffer Descriptors per channel to avoid potential data under/over-flows due to software introduced latency
- No Buffer wrapping
- Buffer size may be equal to, greater than, or less than the packet size. Transfers can automatically switch between buffers.
- Maskable interrupt generation
- Internal arbitration between DMA Channels and external bus arbiter.
- For DMA Data transfer sizes, byte, word and quad-word data transfers are supported.

A set of control and status registers are available to the system processor for setting up DMA operations and monitoring their status. A system interrupt is generated when any or all of the DMA channels wish to inform the processor that a new buffer needs to be allocated. The DMA controller services three peripherals using ten DMA channels, each with its own peripheral DMA bus capable of transferring data in both directions simultaneously.

The MMC and USB peripherals each use two DMA channels, one for transmit and one for receive. The AC97 peripheral uses six DMA channels (three transmit and three receive) to allow different sample frequency data queues to be handled with low software overheads. The DMA Controller does not support memory to memory transfers.

USB Device

The features of the USB are:

- Fully compliant to USB 1.1 specification
- Provides a high level interface that shields the firmware from USB protocol details
- Compatible with both OpenHCI and Intel's UHCI standards
- Supports full-speed (12 Mbps) functions
- Supports Suspend and Resume signalling.

Color LCD Controller

The LH7A400's LCD Controller is programmable to support up to 1,024 × 768, 16-bit color LCD panels. It interfaces directly to STN, color STN, TFT, AD-TFT, and HR-TFT panels. Unlike other LCD controllers, the LH7A400's LCD Controller incorporates the timing conversion logic from TFT to HR- and AD-TFT, allowing a direct interface to these panels and minimizing external chip count.

The Color LCD Controller features support for:

- Up to 1,024 × 768 Resolution
- 16-bit Video Bus
- STN, Color STN, AD-TFT, HR-TFT, TFT panels
- Single and Dual Scan STN panels
- Up to 15 Gray Shades
- Up to 64,000 Colors

AC97 Advanced Audio Codec Interface

The AC97 Advanced Audio Codec controller includes a 5-pin serial interface to an external audio codec. The AC97 LINK is a bi-directional, fixed rate, serial Pulse Code Modulation (PCM) digital stream, dividing each audio frame into 12 outgoing and 12 incoming data streams (slots), each with 20-bit sample resolution.

The AC97 controller contains logic that controls the AC97 link to the Audio Codec and an interface to the AMBA APB.

Its main features include:

- Serial-to-parallel conversion for data received from the external codec
- Parallel-to-serial conversion for data transmitted to the external codec
- Reception/Transmission of control and status information via the AMBA APB interface
- Supports up to 4 different codec sampling rates at a time with its 4 transmit and 4 receive channels. The transmit and receive paths are buffered with internal FIFO memories, allowing data to be stored independently in both transmit and receive modes. The outgoing data for the FIFOs can be written via either the APB interface or with DMA channels 1 - 3.

Audio Codec Interface (ACI)

The ACI provides:

- A digital serial interface to an off-chip 8-bit CODEC
- All the necessary clocks and timing pulses to perform serialization or de-serialization of the data stream to or from the CODEC device.

The interface supports full duplex operation and the transmit and receive paths are buffered with internal FIFO memories allowing up to 16 bytes to be stored independently in both transmit and receive modes.

The ACI includes a programmable frequency divider that generates a common transmit and receive bit clock output from the on-chip ACI clock input (ACICLK). Transmit data values are output synchronous with the rising edge of the bit clock output. Receive data values are sampled on the falling edge of the bit clock output. The start of a data frame is indicated by a synchronization output signal that is synchronous with the bit clock.

Synchronous Serial Port (SSP)

The LH7A400 SSP is a master-only interface for synchronous serial communication with device peripheral devices that has either Motorola SPI, National Semiconductor MICROWIRE or Texas Instruments Synchronous Serial Interfaces.

The LH7A400 SSP performs serial-to-parallel conversion on data received from a peripheral device. The transmit and receive paths are buffered with internal FIFO memories allowing up to eight 16-bit values to be stored independently in both transmit and receive modes. Serial data is transmitted on SSPTXD and received on SSPRXD.

The LH7A400 SSP includes a programmable bit rate clock divider and prescaler to generate the serial output clock SCLK from the input clock SSPCLK. Bit rates are supported to 2 MHz and beyond, subject to choice of frequency for SSPCLK; the maximum bit rate will usually be determined by peripheral devices.

UART/IrDA

The LH7A400 contains three UARTs, UART1, UART2, and UART3.

The UART performs:

- Serial-to-Parallel conversion on data received from the peripheral device
- Parallel-to-Serial conversion on data transmitted to the peripheral device.

The transmit and receive paths are buffered with internal FIFO memories allowing up to 16 bytes to be stored independently in both transmit and receive modes.

The UART can generate:

- Four individually maskable interrupts from the receive, transmit and modem status logic blocks
- A single combined interrupt so that the output is asserted if any of the individual interrupts are asserted and unmasked.

If a framing, parity, or break error occurs during reception, the appropriate error bit is set, and is stored in the FIFO. If an overrun condition occurs, the overrun register bit is set immediately and the FIFO data is prevented from being overwritten. UART1 also supports IrDA 1.0 (15.2 kbit/s).

The modem status input signals Clear to Send (CTS), Data Carrier Detect (DCD) and Data Set Ready (DSR) are supported on UART2 and UART3.

Timers

Two identical timers are integrated in the LH7A400. Each of these timers has an associated 16-bit read/write data register and a control register. Each timer is loaded with the value written to the data register immediately, this value will then be decremented on the next active clock edge to arrive after the write. When the timer underflows, it will immediately assert its appropriate interrupt. The timers can be read at any time. The clock source and mode is selectable by writing to various bits in the system control register. Clock sources are 508 kHz and 2 kHz.

Timer 3 (TC3) has the same basic operation, but is clocked from a single 7.3728 MHz source. It has the same register arrangement as Timer 1 and Timer 2, providing a load, value, control and clear register. Once the timer has been enabled and is written to, unlike the Timer 1 and Timer 2, will decrement the timer on the next rising edge of the 7.3728 MHz clock after the data register has been updated. All the timers can operate in two modes, free running mode or pre-scale mode.

FREE-RUNNING MODE

In free-running mode, the timer will wrap around to 0xFFFF when it underflows and continue counting down.

PRE-SCALE MODE

In pre-scale (periodic) mode, the value written to each timer is automatically re-loaded when the timer underflows. This mode can be used to produce a programmable frequency to drive an external buzzer or generate a periodic interrupt.

Real Time Clock (RTC)

The RTC can be used to provide a basic alarm function or long time-base counter. This is achieved by generating an interrupt signal after counting for a programmed number of cycles of a real-time clock input. Counting in one second intervals is achieved by use of a 1 Hz clock input to the RTC.

Battery Monitor Interface (BMI)

The LH7A400 BMI is a serial communication interface specified for two types of Battery Monitors/Gas Gauges. The first type employs a single wire interface. The second interface employs a two-wire multi-master bus, the Smart Battery System Specification. If both interfaces are enabled at the same time, the Single Wire Interface will have priority. A brief overview of these two interface types are given here.

SINGLE WIRE INTERFACE

The Single Wire Interface performs:

- Serial-to-parallel conversion on data received from the peripheral device
- Parallel-to-serial conversion on data transmitted to the peripheral device
- Data packet coding/decoding on data transfers (incorporating Start/Data/Stop data packets)

The Single Wire interface uses a command-based protocol, in which the host initiates a data transfer by sending a WriteData/Command word to the Battery Monitor. This word will always contain the Command section, which tells the Single Wire Interface device the location for the current transaction. The most significant bit of the Command determines if the transaction is Read or Write. In the case of a Write transaction, then the word will also contain a WriteData section with the data to be written to the peripheral.

SMART BATTERY INTERFACE

The SMBus Interface performs:

- Serial-to-Parallel conversion on data received from the peripheral device
- Parallel-to-Serial conversion of data transmitted to the peripheral device.

The Smart Battery Interface uses a two-wire multi-master bus (the SMBus), meaning that more than one device capable of controlling the bus can be connected to it. A master device initiates a bus transfer and provides the clock signals. A slave device can receive data provided by the master or it can provide data to the master. Since more than one device may attempt to take control of the bus as a master, SMBus provides an arbitration mechanism, by relying on the wired-AND connection of all SMBus interfaces to the SMBus.

DC-to-DC Converter

The features of the DC-DC Converter interface are:

- Dual drive PWM outputs, with independent closed loop feedback
- Software programmable configuration of one of 8 output frequencies (each being a fixed divide of the input clock).
- Software programmable configuration of duty cycle from 0 to 15/16, in intervals of 1/16.
- Output polarity (for positive or negative voltage generation) is hardware-configured during power-on reset via the polarity select inputs
- Each PWM output can be dynamically switched to one of a pair of preprogrammed frequency/duty cycle combinations via external pins.

Watchdog Timer (WDT)

The Watchdog Timer provides hardware protection against malfunctions. It is a programmable timer that is reset by software at regular intervals. Failure to reset the timer will cause a FIQ interrupt. Failure to service the FIQ interrupt will then generate a System Reset. The WDT features are:

- Driven by the system clock
- 16 programmable time-out periods: 2^{16} through 2^{31} clock cycles
- Generates a system reset (resets LH7A400) or a FIQ Interrupt whenever a time-out period is reached
- Software enable, lockout, and counter-reset mechanisms add security against inadvertent writes
- Protection mechanism guards against interrupt-service-failure:
  - The first WDT time-out triggers FIQ and asserts nWDFIQ status flag
  - If FIQ service routine fails to clear nWDFIQ, then the next WDT time-out triggers a System Reset.

General Purpose I/O (GPIO)

The LH7A400 GPIO has eight ports, each with a data register and a data direction register. It also has added registers including Keyboard Scan, PINMUX, GPIO Interrupt Enable, INTYPE1/2, GPIOFEOI, and PGHCON.

The data direction register determines whether a port is configured as an input or an output while the data register is used to read the value of the GPIO pins.

The GPIO Interrupt Enable, INTYPE1/2, and GPIOFEOI registers are used to control edge-triggered Interrupts on Port F. The PINMUX register controls what signals are output of Port D and Port E when they are set as outputs, while the PGHCON controls the operations of Port G and H.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

PARAMETER	MINIMUM	MAXIMUM
DC Core Supply Voltage (VDDC)	–0.3 V	2.4 V
DC I/O Supply Voltage (VDD)	–0.3 V	4.6 V
DC Analog Supply Voltage (VDDA)	–0.3 V	2.4 V
5 V Tolerant Digital Input Pin Voltage	–0.5 V	5.5 V
ESD, Human Body Model (Analog pins AN0 - AN9 rated at 500 V)		2 kV
ESD, Charged Device Model		1 kV
Storage Temperature	–55°C	125°C

NOTE: Except for Storage Temperature, these ratings are only for transient conditions. Operation at or beyond absolute maximum rating conditions may affect reliability and cause permanent damage to the device.

Recommended Operating Conditions

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	NOTES
DC Core Supply Voltage (VDDC)	1.71 V	1.8 V	1.89 V	1, 4
DC Core Supply Voltage (VDDC)	2.0 V	2.1 V	2.2 V	1, 5
DC I/O Supply Voltage (VDD)	3.0 V	3.3 V	3.6 V	2, 6
DC I/O Supply Voltage (VDD)	3.14 V	3.3 V	3.6 V	2, 7
DC Analog Supply Voltage for PLLs (VDDA)	1.71 V	1.8 V	1.89 V	
Clock Frequency (0°C to +70°C)	10 MHz		200 MHz	3, 4, 6
Clock Frequency (–40°C to +85°C)	10 MHz		195 MHz	3, 4, 6
Bus Clock Frequency (–40°C to +85°C)			100 MHz	3, 4, 6
Clock Frequency (0°C to +70°C)	10 MHz		250 MHz	3, 5, 7
Clock Frequency (–40°C to +85°C)	10 MHz		245 MHz	3, 5, 7
Bus Clock Frequency (–40°C to +85°C)			125 MHz	3, 5, 7
External Clock Input (XTALIN)	14 MHz	14.7456 MHz	20 MHz	8
External Clock Input (XTALIN) Voltage	1.71 V	1.8 V	1.89 V	
Operating Temperature	–40°C	25°C	+85°C	

NOTES:
1. Core Voltage should never exceed I/O Voltage after initial power up. See “Power Supply Sequencing” on page 33
2. USB is not functional below 3.0 V
3. Using 14.7456 MHz Main Oscillator Crystal and 32.768 kHz RTC Oscillator Crystal
4. VDDC = 1.71 V to 1.89 V (LH7A400N0G000xx)
5. VDDC = 2.1 V ± 5 % (LH7A400N0G076xx only)
6. VDD = 3.0 V to 3.6 V (LH7A400N0G000xx)
7. VDD = 3.14V to 3.60 V (LH7A400N0G076xx only)
8. IMPORTANT: Most peripherals will NOT function with crystals other than 14.7456 MHz.

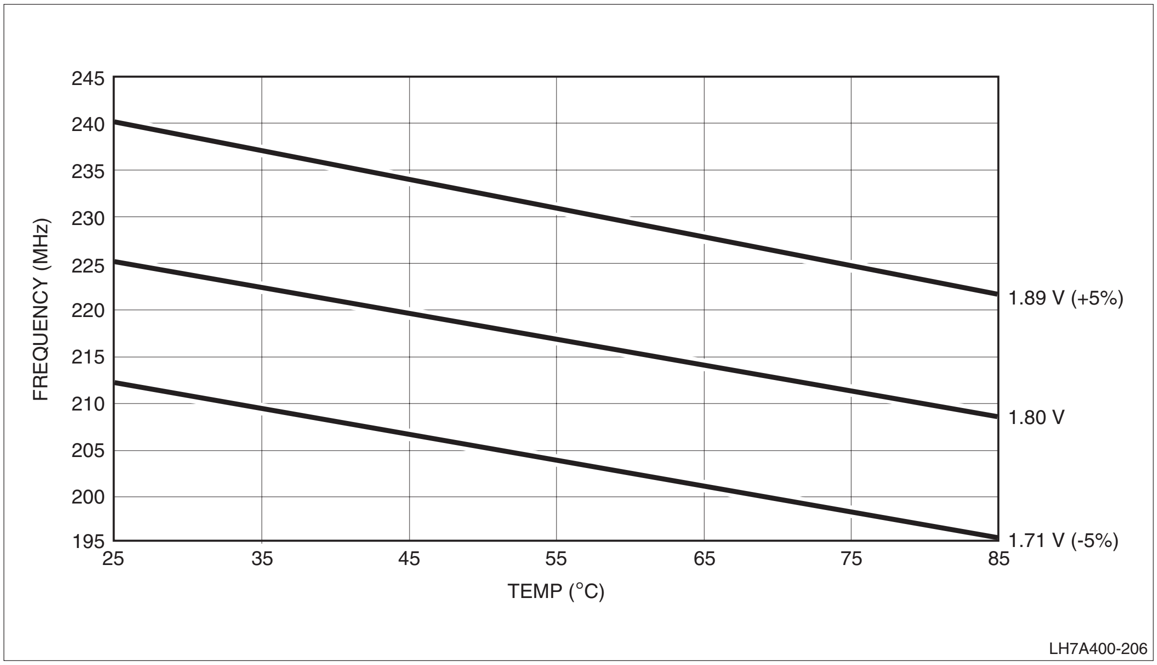


Figure 8. Temperature/Voltage/Speed Chart (For LH7A400N0G000xx)

Table 9. Clock Frequency vs. Voltages (VDDC) vs. Temperature

PARAMETER		1.71 V	1.8 V	1.89 V
25°C	Clock Frequency (FCLK)	211 MHz	225 MHz	240 MHz
	Clock Period (FCLK)	4.74 ns	4.44 ns	4.17 ns
70°C	Clock Frequency (FCLK)	200 MHz	212 MHz	227 MHz
	Clock Period (FCLK)	5.00 ns	4.72 ns	4.41 ns
85°C	Clock Frequency (FCLK)	195 MHz	208 MHz	222 MHz
	Clock Period (FCLK)	5.13 ns	4.81 ns	4.50 ns

NOTES:
1. Table 9 is representative of a typical wafer process. Guaranteed values are in the Recommended Operating Conditions table.
2. LH7A400N0G000xx

DC/AC SPECIFICATIONS

Unless otherwise noted, all data provided in these specifications are based on –40°C to +85°C, VDDC = 1.71 V to 1.89 V, VDD = 3.0 V to 3.6 V, VDDA = 1.71 V to 1.89 V.

DC Specifications

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS	NOTES
VIH	CMOS and Schmitt Trigger Input HIGH Voltage	2.0		5.5	V		
VIL	CMOS and Schmitt Trigger Input LOW Voltage	–0.2		0.8	V		
VHST	Schmitt Trigger Hysteresis	0.25			V	VIL to VIH	
VOH	Output Drive 2	2.6			V	IOH = –4 mA	
	Output Drive 3	2.6			V	IOH = –8 mA	
	Output Drive 4 and 5	2.6			V	IOH = –12 mA	1
VOL	Output Drive 2			0.4	V	IOL = 4 mA	
	Output Drive 3			0.4	V	IOL = 8 mA	
	Output Drive 4			0.4	V	IOL = 12 mA	
	Output Drive 5			0.4	V	IOL = 20 mA	1
IIN	Input Leakage Current	–10		10	μA	VIN = VDD or GND	
	Input Leakage Current (with pull-up resistors installed)	–200		–20	μA	VIN = VDD or GND	
IOZ	Output Tri-state Leakage Current	–10		10	μA	VOUT = VDD or GND	
ISTARTUP	Startup Current			50	μA		2
IACTIVE	Active Current		125	180	mA		
IHALT	Halt Current		25	41	mA		
ISTANDBY	Standby Current		42		μA		
CIN	Input Capacitance			4	pF		
COUT	Output Capacitance			4	pF		

NOTES:
1. Output Drive 5 can sink 20 mA of current, but sources 12 mA of current.
2. Current consumption until oscillators are stabilized.

AC Test Conditions

PARAMETER	RATING	UNIT
DC I/O Supply Voltage (VDD)	3.0 to 3.6	V
DC Core Supply Voltage (VDDC)	1.71 to 1.89	V
Input Pulse Levels	VSS to 3	V
Input Rise and Fall Times	2	ns
Input and Output Timing Reference Levels	VDD/2	V

CURRENT CONSUMPTION BY OPERATING MODE

Current consumption can depend on a number of parameters. To make this data more usable, the values presented in Table 10 were derived under the conditions presented here.

Maximum Specified Value

The values specified in the MAXIMUM column were determined using these operating characteristics:

- All IP blocks either operating or enabled at maximum frequency and size configuration
- Core operating at maximum power configuration
- All voltages at maximum specified values
- Maximum specified ambient temperature (tAMB).

Typical

The values in the TYPICAL column were determined using a ‘typical’ application under ‘typical’ environmental conditions and the following operating characteristics:

- LINUX operating system running from SDRAM
- UART and AC97 peripherals operating; all other peripherals as needed by the OS
- LCD enabled with 320 × 240 × 16-bit color, 60 Hz refresh rate, data in SDRAM
- I/O loads at nominal
- Cache enabled
- FCLK = 200 MHz or 250 MHz; HCLK = 100 MHz or 125 MHz; PCLK = 50 MHz or 62.5 MHz
- All voltages at typical values
- Nominal case temperature (tAMB).

Table 10. Current Consumption by Mode

SYMBOL	PARAMETER	LH7A400N0G000xx (FCLK = 200 MHz)		LH7A400N0G076xx (FCLK = 250 MHz)	
		TYP.	MAX.	TYP.	UNITS
ACTIVE MODE					
ICORE	Core Current	110	135	250	mA
IIO	I/ O Current	15	45		mA
HALT MODE (ALL PERIPHERALS DISABLED)					
ICORE	Core Current	24	39	50	mA
IIO	I/ O Current	1	2		mA
STANDBY MODE (TYPICAL CONDITIONS ONLY)					
ICORE	Core Current	40		125	µA
IIO	I/ O Current	2		4	µA

PERIPHERAL CURRENT CONSUMPTION

In addition to the modal current consumption, Table 11 shows the typical current consumption for each of the on-board peripheral blocks. The values were determined with the CPU clock running at 200 MHz, typical conditions, and no I/O loads. This current is supplied by the 1.8 VDDC power supply.

Table 11. Peripheral Current Consumption

PERIPHERAL	TYPICAL	UNITS
AC97	1.3	mA
UART (Each)	1.0	mA
RTC	0.005	mA
Timers (Each)	0.1	mA
LCD (+I/O)	5.4 (1.0)	mA
MMC	0.6	mA
SCI	23	mA
PWM (each)	< 0.1	mA
BMI-SWI	1.0	mA
BMI-SBus	1.0	mA
SDRAM (+I/O)	1.5 (14.8)	mA
USB (+PLL)	5.6 (3.3)	mA
ACI	0.8	mA

Power Supply Sequencing

NXP recommends that the 1.8 V power supply be energized before the 3.3 V supply. If this is not possible, the 1.8 V supply may not lag the 3.3 V supply by more than 100 µs. If longer delay time is needed, it is recommended that the voltage difference between the two power supplies be within 1.5 V during power supply ramp up.

To avoid a potential latchup condition, voltage should be applied to input pins only after the device is powered-on as described above.

AC Specifications

All signals described in Table 12 relate to transitions after a reference clock signal. The illustration in Figure 9 represents all cases of these sets of measurement parameters.

The reference clock signals in this design are:

- HCLK, internal System Bus clock (‘C’ in timing data)
- PCLK, Peripheral Bus clock
- SSPCLK, Synchronous Serial Port clock
- UARTCLK, UART Interface clock
- LCDDCLK, LCD Data clock from the LCD Controller
- ACBITCLK, AC97 clock
- SCLK, Synchronous Memory clock.

All signal transitions are measured at the 50 % point.

For outputs from the LH7A400, tOVXXX (e.g. tOVA) represents the amount of time for the output to become valid from a valid address bus, or rising edge of the peripheral clock. Maximum requirements for tOVXXX are shown in Table 12.

The signal tOHXXX (e.g. tOHA) represents the amount of time the output will be held valid from the valid address bus, or rising edge of the peripheral clock. Minimum requirements for tOHXXX are listed in Table 12.

For Inputs, tISXXX (e.g. tISD) represents the amount of time the input signal must be valid before a valid address bus, or rising edge of the peripheral clock (except SSP and ACI). Maximum requirements for tISXXX are shown in Table 12.

The signal tIHXXX (e.g. tIHD) represents the amount of time the output must be held valid from the valid address bus, or rising edge of the peripheral clock (except SSP and ACI). Minimum requirements are shown in Table 12.

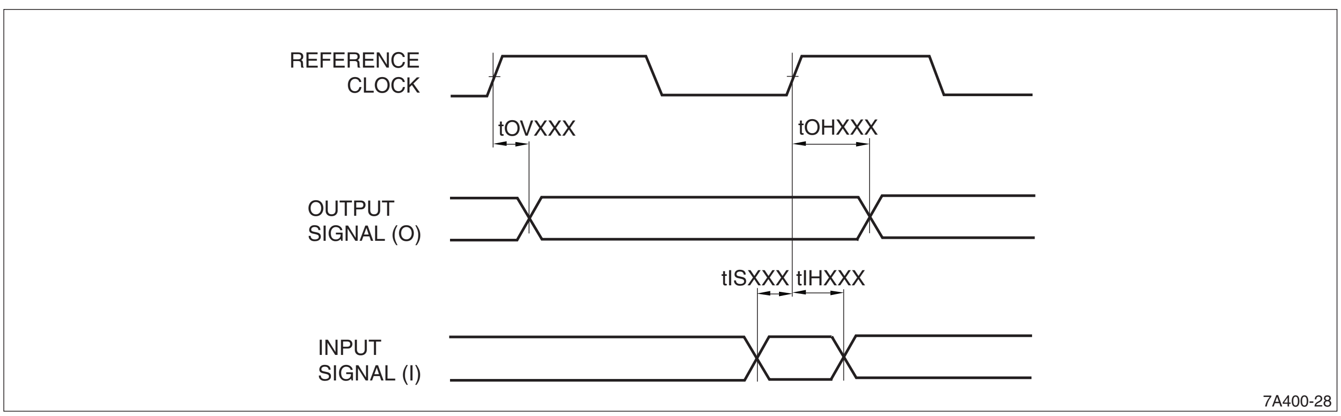


Figure 9. LH7A400 Signal Timing

Table 12. AC Signal Characteristics

SIGNAL	TYPE	LOAD	SYMBOL	MIN.	MAX.	DESCRIPTION
ASYNCHRONOUS MEMORY INTERFACE SIGNALS (+ [wait states × HCLK period])[1]						
A[27:0]	Output	50 pF	tRC	4 × tHCLK – 7.0 ns	4 × tHCLK + 7.5 ns	Read Cycle Time
	Output	50 pF	tWC	4 × tHCLK – 7.0 ns	4 × tHCLK + 7.5 ns	Write Cycle Time
	—	—	tWS	tHCLK ns	tHCLK ns	Wait State Width
D[31:0]	Output	50 pF	tDVWE	tHCLK – 6.0 ns	tHCLK – 2.0 ns	Data Valid to Write Edge (nWE invalid)
			tDHWE	tHCLK – 7.0 ns	tHCLK + 2.0 ns	Data Hold after Write Edge (nWE invalid)
			tDVBE	tHCLK – 5.0 ns	tHCLK – 1.0 ns	Data Valid to nBLE Invalid
			tDHBE	tHCLK – 7.0 ns	tHCLK + 3.0 ns	Data Hold after nBLE Invalid
	Input	—	tDSCS	15 ns	—	Data Setup to nCSx Invalid
			tDHCS	0 ns	—	Data Hold to nCSx Invalid
			tDSOE	15 ns	—	Data Setup to nOE Invalid
			tDHOE	0 ns	—	Data Hold to nOE Invalid
			tDSBE	15 ns	—	Data Setup to nBLE Invalid
			tDHBE	0 ns	—	Data Hold to nBLE Invalid
nCS[7:0]	Output	30 pF	tCS	2 × tHCLK – 3.0 ns	2 × tHCLK + 3.0 ns	nCSx Width
			tAVCS	tHCLK – 4.0 ns	tHCLK	Address Valid to nCSx Valid
			tAHCS	tHCLK	tHCLK + 4.5 ns	Address Hold after nCSx Invalid
SYNCHRONOUS MEMORY INTERFACE SIGNALS						
SA[13:0]	Output	50 pF	tOVA		5.5[3]/7.5[4] ns	Address Valid
			tOHA	1.5[3]/1.5[4] ns		Address Hold
SA[17:16]/SB[1:0]	Output	50 pF	tOVB		5.5[3]/7.5[4] ns	Bank Select Valid
D[31:0]	Output	50 pF	tOHD	1.5ns		Data Hold
			tOVD	2 ns	5.5[3]/7.5[4] ns	Data Valid
	Input		tISD	1.5[3]/2.5[4] ns		Data Setup
			tIHD	1.0[3]/1.5[4] ns		Data Hold
nCAS	Output	30 pF	tOVCA	2 ns	5.5[3]/7.5[4] ns	CAS Valid
			tOHCA	1.5[3]/2[4] ns		CAS Hold
nRAS	Output	30 pF	tOVRA	2 ns	5.5[3]/7.5[4] ns	RAS Valid
			tOHRA	1.5[3]/2[4] ns		RAS Hold
nSWE	Output	30 pF	tOVSDW	2 ns	5.5[3]/7.5[4] ns	Write Enable Valid
			tOHSDW	1.5[3]/2[4] ns		Write Enable Hold
SCKE[1:0]	Output	30 pF	tOVC	2 ns	5.5[3]/7.5[4] ns	Clock Enable Valid
DQM[3:0]	Output	30 pF	tOVDQ	2 ns	5.5[3]/7.5[4] ns	Data Mask Valid
nSCS[3:0]	Output	30 pF	tOVSC	2 ns	5.5[3]/7.5[4] ns	Synchronous Chip Select Valid
			tOHSC	1.5[3]/2[4] ns		Synchronous Chip Select Hold
PCMCIA INTERFACE SIGNALS (+ wait states × HCLK period)						
nPCREG	Output	30 pF	tOVDREG		tHCLK	nREG Valid
			tOHDREG	4 × tHCLK – 5 ns		nREG Hold
D[31:0]	Output	50 pF	tOVD		tHCLK	Data Valid
			tOHD	4 × tHCLK – 5 ns		Data Hold
	Input		tISD		tHCLK - 10 ns	Data Setup Time
			tIHD	4 × tHCLK – 5 ns		Data Hold Time
nPCCE1	Output	30 pF	tOVCE1		tHCLK	Chip Enable 1 Valid
			tOHCE1	4 × tHCLK – 5 ns		Chip Enable 1 Hold
nPCCE2	Output	30 pF	tOVCE2		tHCLK	Chip Enable 2 Valid
			tOHCE2	4 × tHCLK – 5 ns		Chip Enable 2 Hold
nPCOE	Output	30 pF	tOVOE		tHCLK + 1 ns	Output Enable Valid
			tOHOE	3 × tHCLK – 5 ns		Output Enable Hold
nPCWE	Output	30 pF	tOVWE		tHCLK + 1 ns	Write Enable Valid
			tOHWE	3 × tHCLK – 5 ns		Write Enable Hold
PCDIR	Output	30 pF	tOVPCD		tHCLK	Card Direction Valid
			tOHPCD	4 × tHCLK – 5 ns		Card Direction Hold

Table 12. AC Signal Characteristics (Cont'd)

SIGNAL	TYPE	LOAD	SYMBOL	MIN.	MAX.	DESCRIPTION
MMC INTERFACE SIGNALS						
MMCCMD	Output	100 pF	tOS	5 ns		MMC Command Setup
			tOH	5 ns		MMC Command Hold
MMCDATA	Output	100 pF	tOS	5 ns		MMC Data Setup
			tOH	5 ns		MMC Data Hold
MMCDATA	Input		tIS	3 ns		MMC Data Setup
			tIH	3 ns		MMC Data Hold
MMCCMD	Input		tIS	3 ns		MMC Command Setup
			tIH	3 ns		MMC Command Hold
AC97 INTERFACE SIGNALS						
ACOUT/ACSYNC	Output	30 pF	tOVAC97		15 ns	AC97 Output Valid/Sync Valid
			tOHAC97	10 ns		AC97 Output Hold/Sync Hold
ACIN	Input		tISAC97	10 ns		AC97 Input Setup
			tIHAC97	2.5 ns		AC97 Input Hold
ACBITCLK	Input		tACBITCLK	72 ns	90 ns	AC97 Clock Period
SYNCHRONOUS SERIAL PORT (SSP)						
SSPFRM	Output		tOVSSPFRM		10 ns	SSPFRM Valid
			tOHSSPFRM	5 ns		SSPFRM Hold
SSPTX	Output	50 pF	tOVSSPOUT		10 ns	SSP Transmit Valid
			tOHSSPOUT	5 ns		SSP Transmit Hold
SSPRX	Input		tISSSPIN	14 ns		SSP Receive Setup
SSPCLK	Output		tSSPCLK	8.819 ms	271 ns	SSP Clock Period
AUDIO CODEC INTERFACE (ACI)						
ACOUT	Output	30 pF	tOVD		15 ns	ACOUT delay from rising clock edge
			tOHD	10 ns		ACOUT Hold
ACIN	Input		tIS	10 ns		ACIN Setup
			tIH	2.5 ns		ACIN Hold
COLOR LCD CONTROLLER						
LCDVD [17:0]	Output	30 pF	tOV	—	3 ns	LCD Data Clock to Data Valid

NOTES:
1. Register BCRx:WST1 = 0b000
2. For Output Drive strength specifications, refer to Table 3
3. LH7A400N0G076xx only
4. LH7A400N0G000xx only

SMC Waveforms

Figure 10 and Figure 11 show the waveform and timing for an External Asynchronous Memory Write. Note that the deassertion of nWE can precede the deassertion of nCS by a maximum of one HCLK, or at minimum, can coincide (see Table 12). Figure 12 and Figure 13 show the waveform and timing for an External Asynchronous Memory Read.

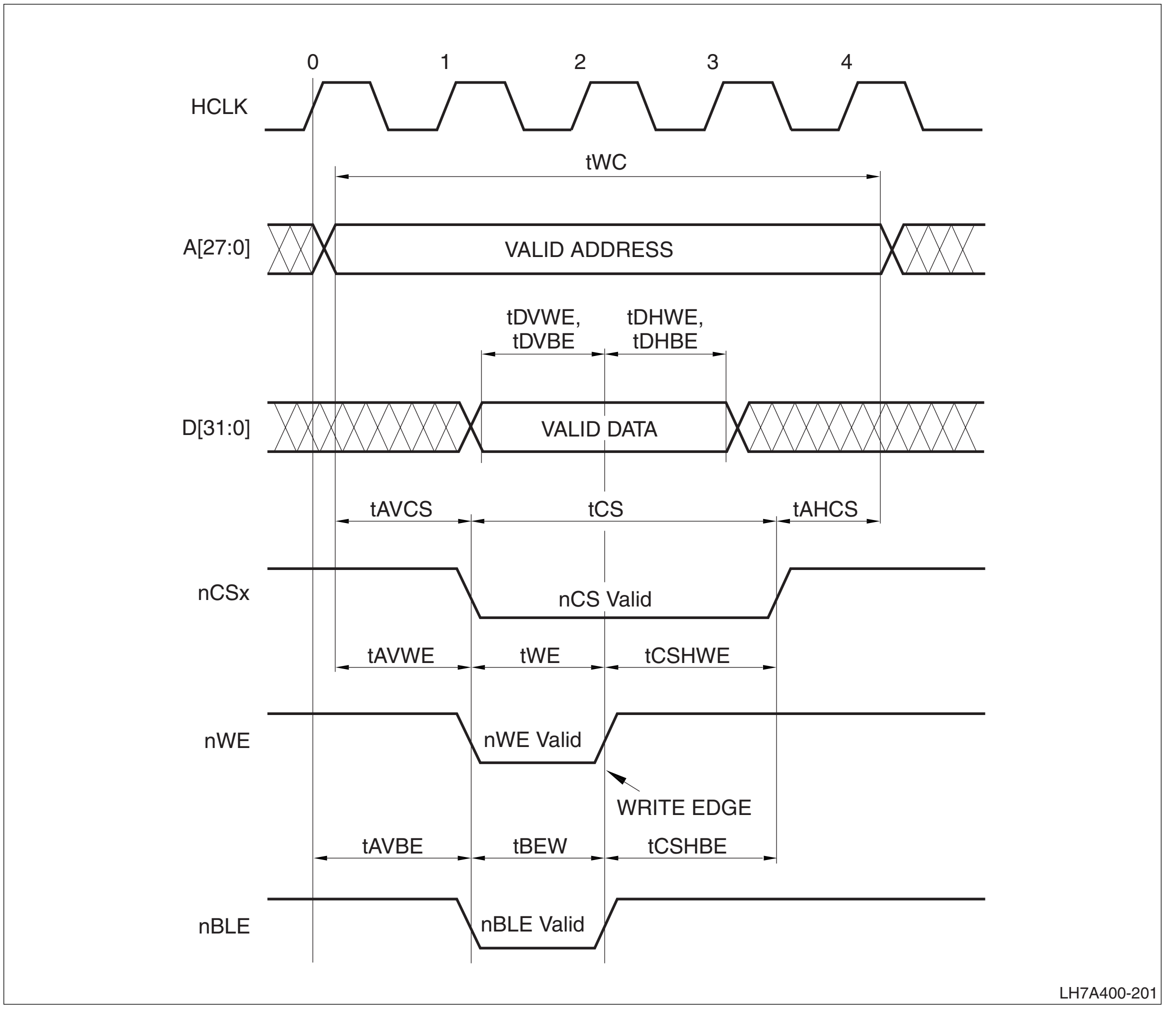


Figure 10. External Asynchronous Memory Write with 0 Wait States (BCRx:WST1 = 0b000)

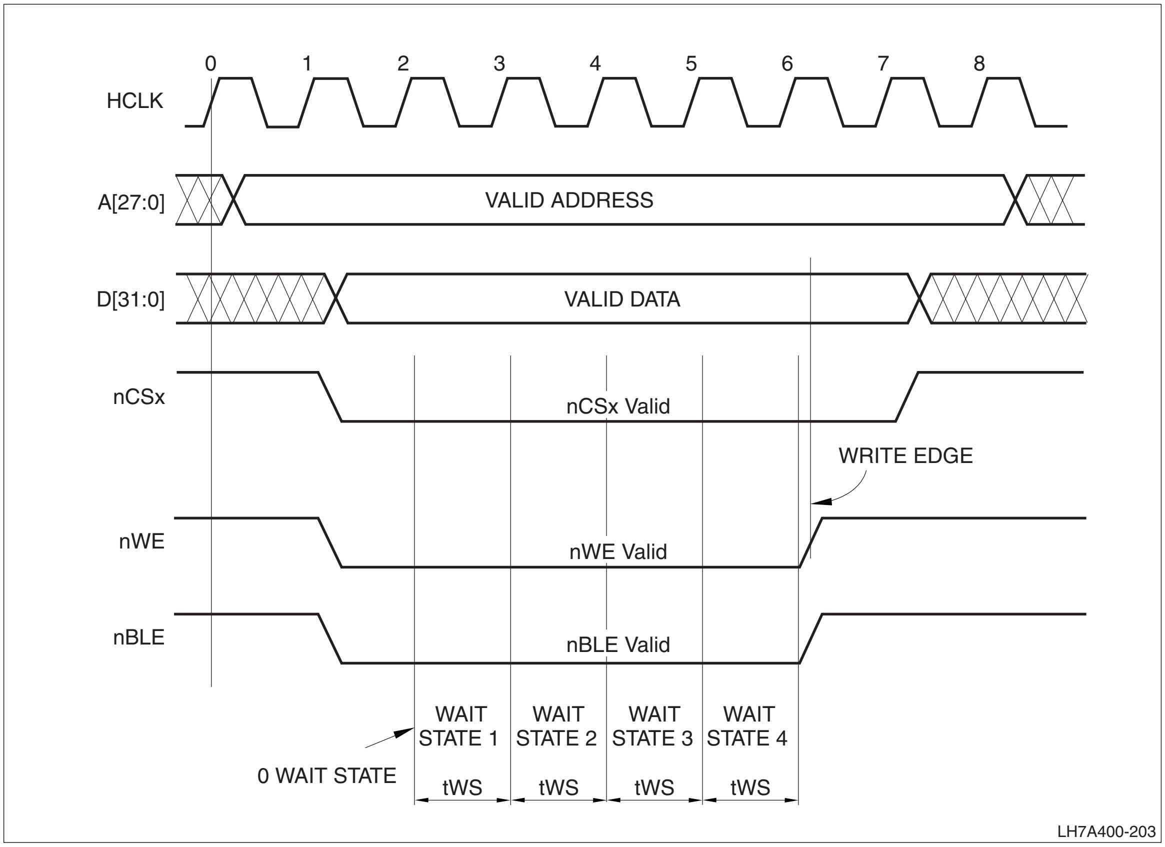


Figure 11. External Asynchronous Memory Write with 4 Wait States (BCRx:WST1 = 0b100)

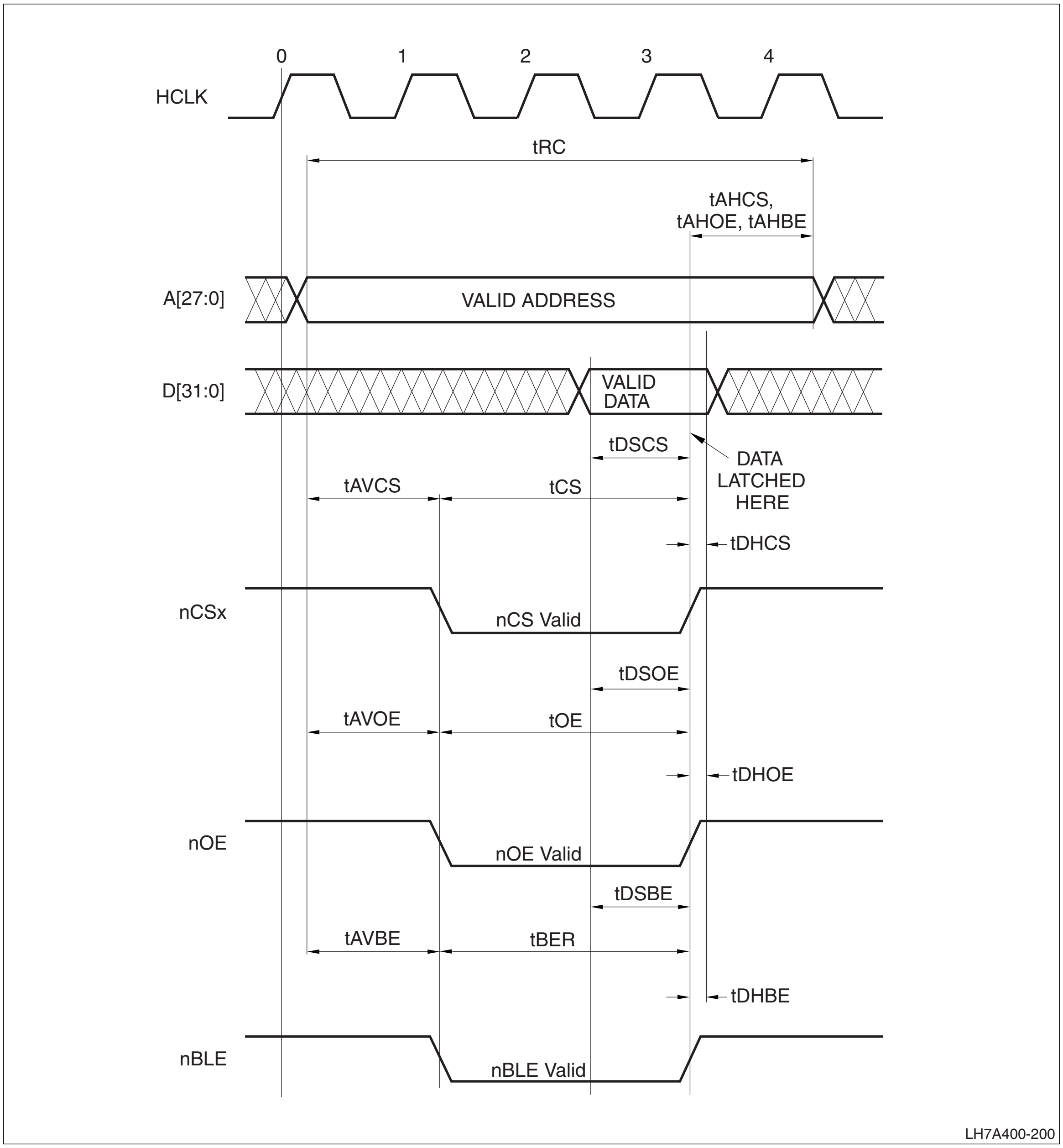


Figure 12. External Asynchronous Memory Read with 0 Wait States (BCRx:WST1 = 0b000)

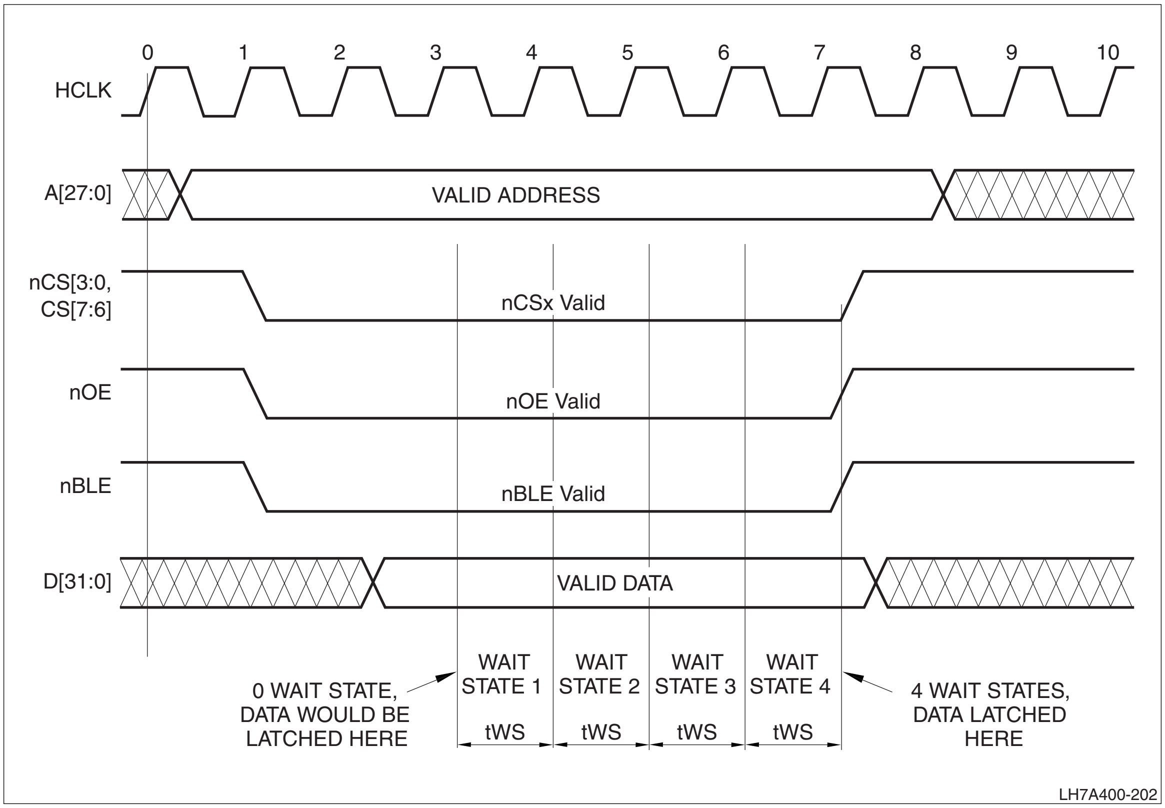


Figure 13. External Asynchronous Memory Read with 4 Wait States (BCRx:WST1 = 0b100)

Synchronous Memory Controller Waveforms

Figure 14 shows the timing for a Synchronous Burst Read (page already open). Figure 15 shows the timing for Activate a Bank and Write.

SSP Waveforms

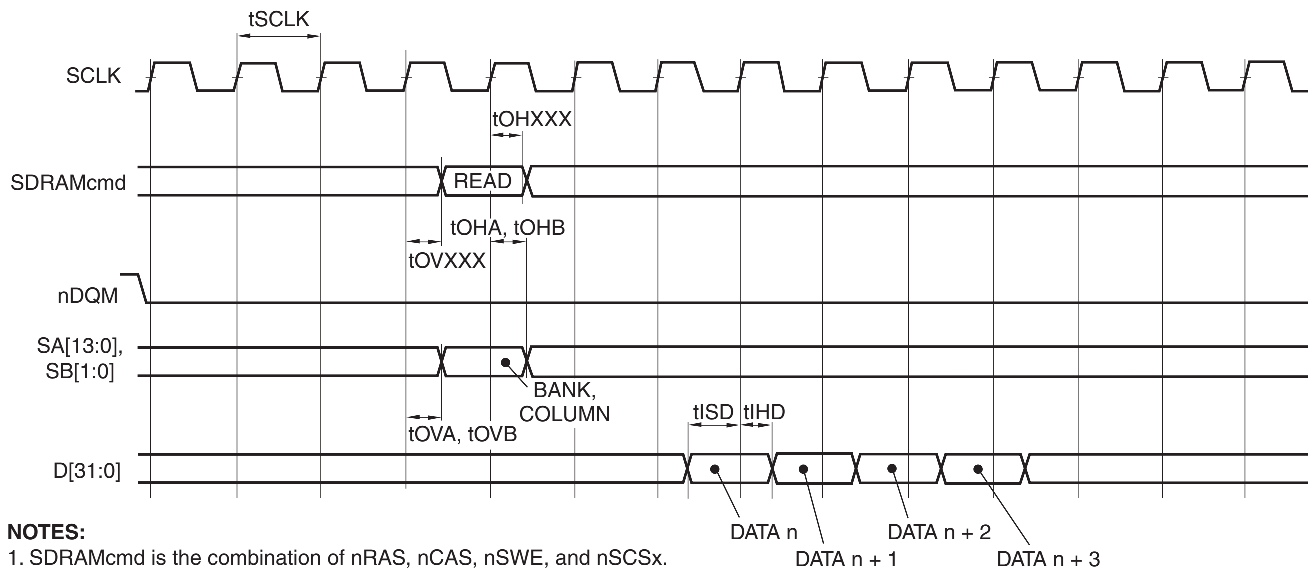
The Synchronous Serial Port (SSP) supports three data frame formats:

- Texas Instruments SSI
- Motorola SPI
- National Semiconductor MICROWIRE

Each frame format is between 4 and 16 bits in length, depending upon the programmed data size. Each data frame is transmitted beginning with the Most Significant Bit (MSB) i.e. ‘big endian’. For all three formats, the SSP serial clock is held LOW (inactive) while the SSP is idle. The SSP serial clock transitions only during active transmission of data. The SSPFRM signal marks the beginning and end of a frame. The SSPEN signal controls an off-chip line driver’s output enable pin.

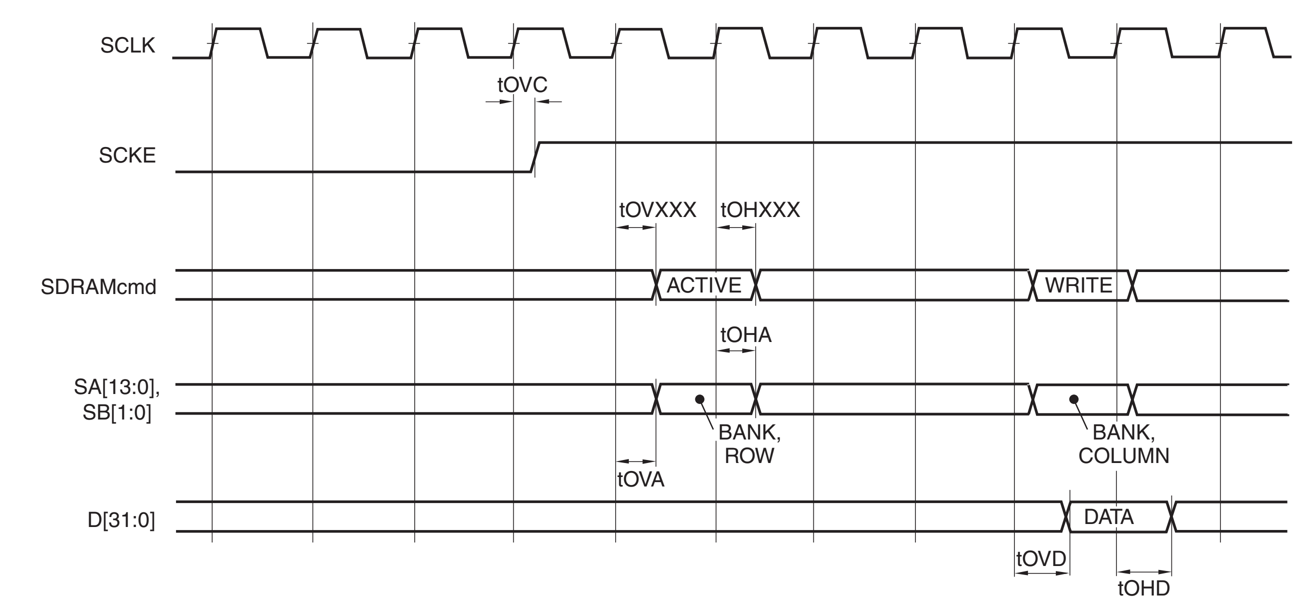
Figure 16 and Figure 17 show Texas Instruments synchronous serial frame format, Figure 18 through Figure 25 show the Motorola SPI format, and Figure 26 and Figure 27 show National Semiconductor’s MICROWIRE data frame format.

For Texas Instruments SSI format, the SSPFRM pin is pulsed prior to each frame’s transmission for one serial clock period beginning at its rising edge. For this frame format, both the SSP and the external slave device drive their output data on the rising edge of the clock and latch data from the other device on the falling edge. See Figure 16 and Figure 17.



NOTES:
1. SDRAMcmd is the combination of nRAS, nCAS, nSWE, and nSCSx.
2. tOVXXX represents tOVRA, tOVCA, tOVSVW, or tOVSC.
3. tOHXXX represents tOHRA, tOHCA, tOHSVW, or tOHSC.
4. DQM[3:0] is static LOW.
5. SCKE is static HIGH.

Figure 14. Synchronous Burst Read



NOTES:
1. SDRAMcmd is the combination of nRAS, nCAS, nSWE, and nSCSx.
2. tOVXXX represents tOVRA, tOVCA, tOVSVW, or tOVSC. Refer to the AC timing table.
3. tOHXXX represents tOHRA, tOHCA, tOHSVW, or tOHSC.

Figure 15. Synchronous Bank Activate and Write

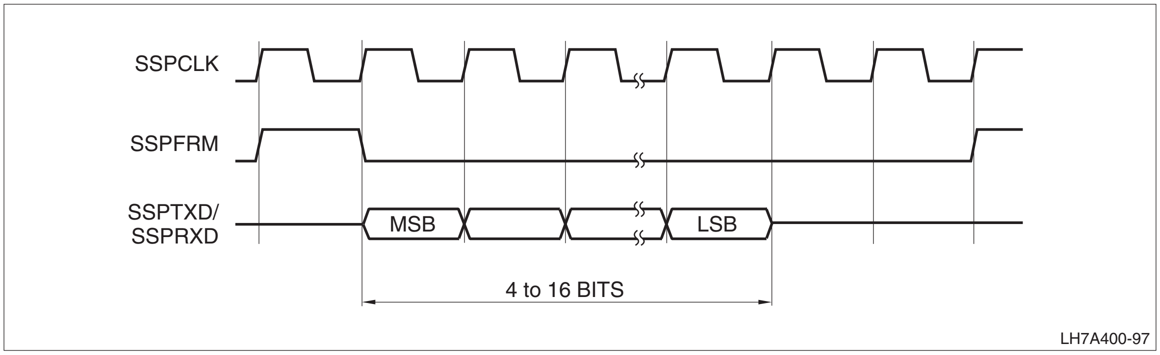


Figure 16. Texas Instruments Synchronous Serial Frame Format (Single Transfer)

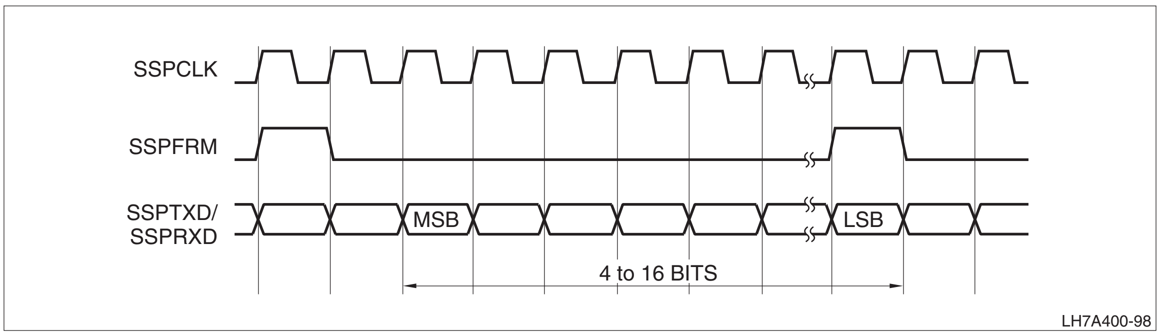


Figure 17. Texas Instruments Synchronous Serial Frame Format (Continuous Transfer)

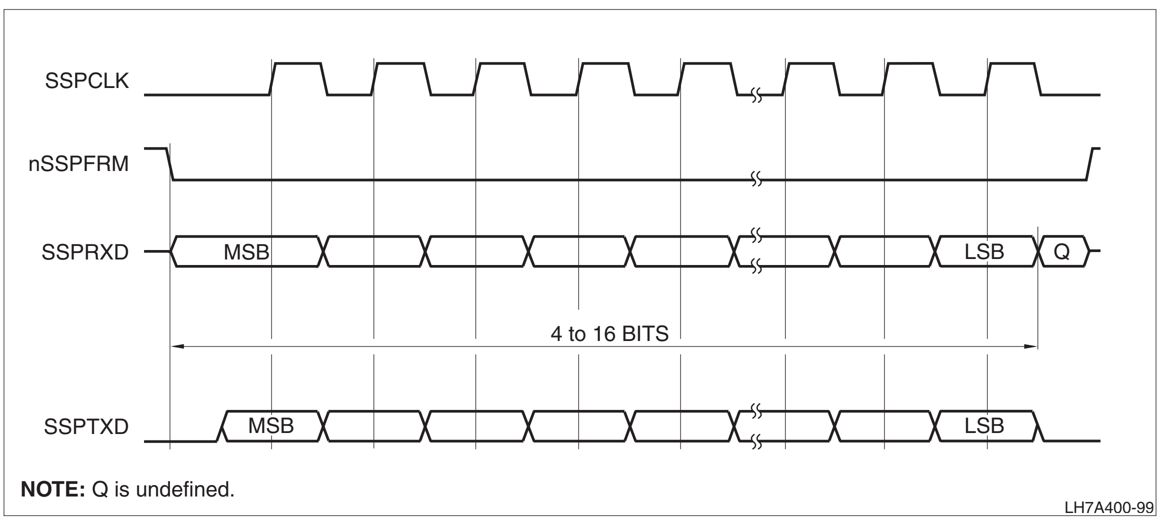


Figure 18. Motorola SPI Frame Format (Single Transfer) with SPO = 0 and SPH = 0

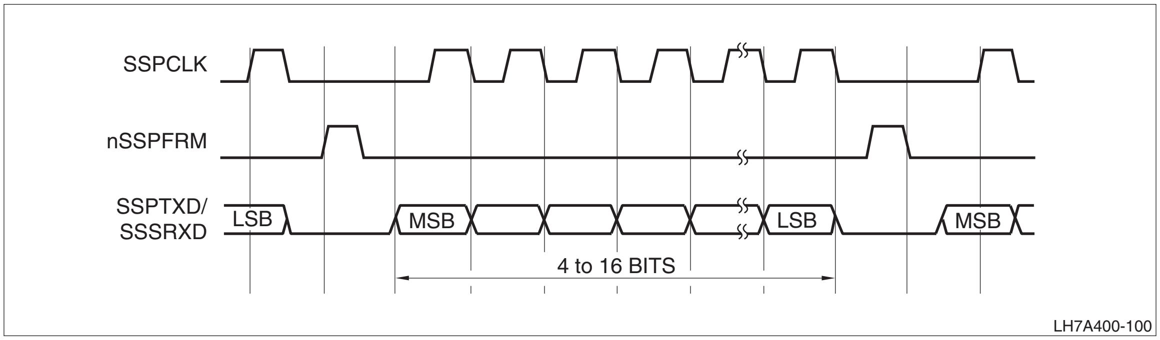


Figure 19. Motorola SPI Frame Format (Continuous Transfer) with SPO = 0 and SPH = 0

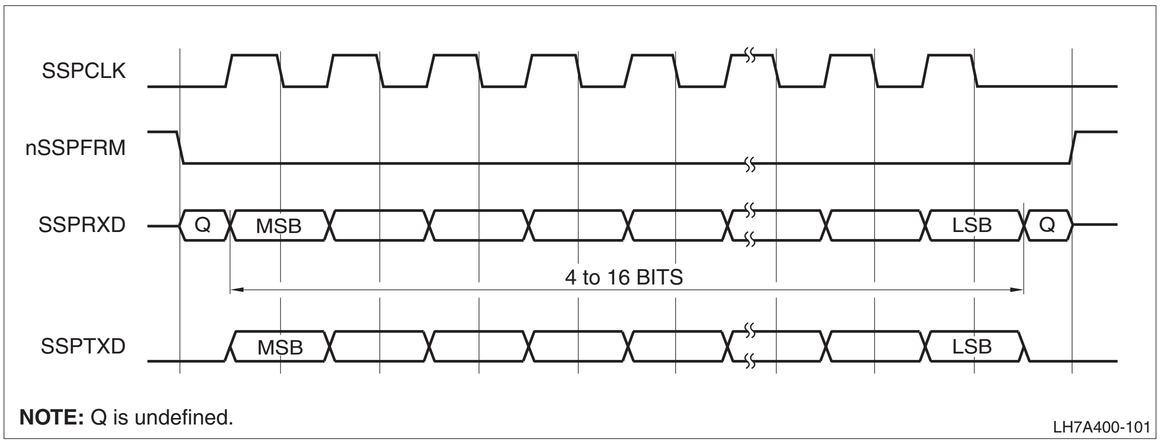


Figure 20. Motorola SPI Frame Format (Single Transfer) with SPO = 0 and SPH = 1

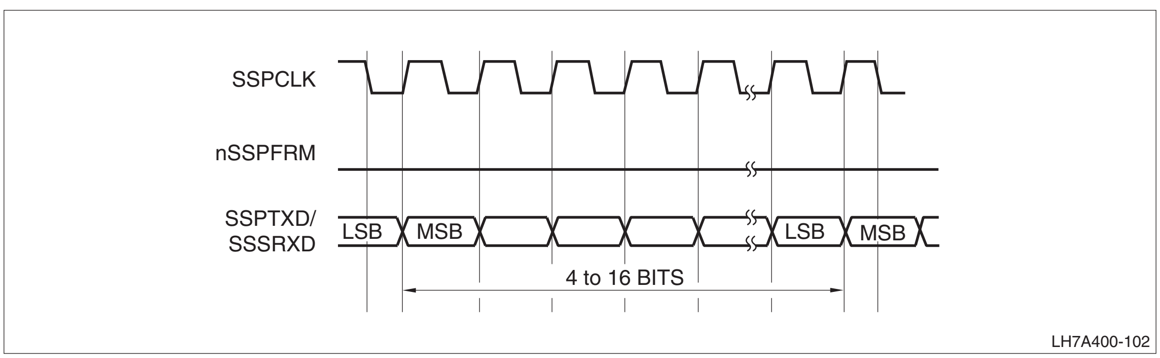


Figure 21. Motorola SPI Frame Format (Continuous Transfer) with SPO = 0 and SPH = 1

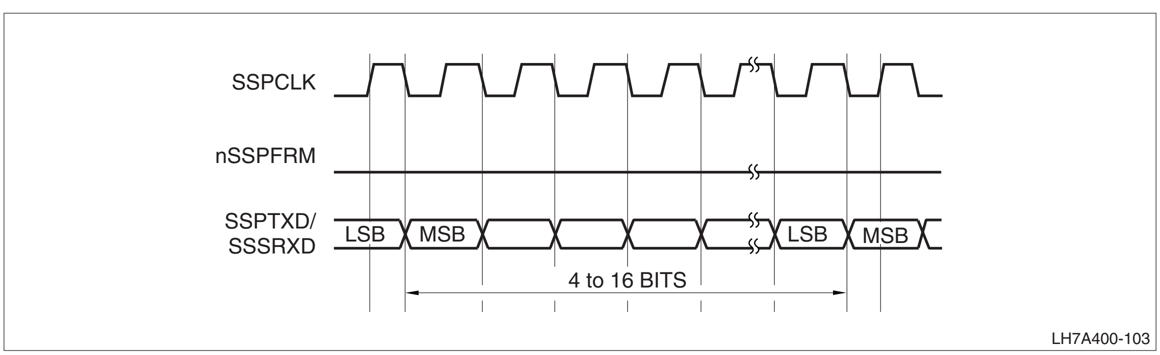


Figure 22. Motorola SPI Frame Format (Continuous Transfer) with SPO = 1 and SPH = 1

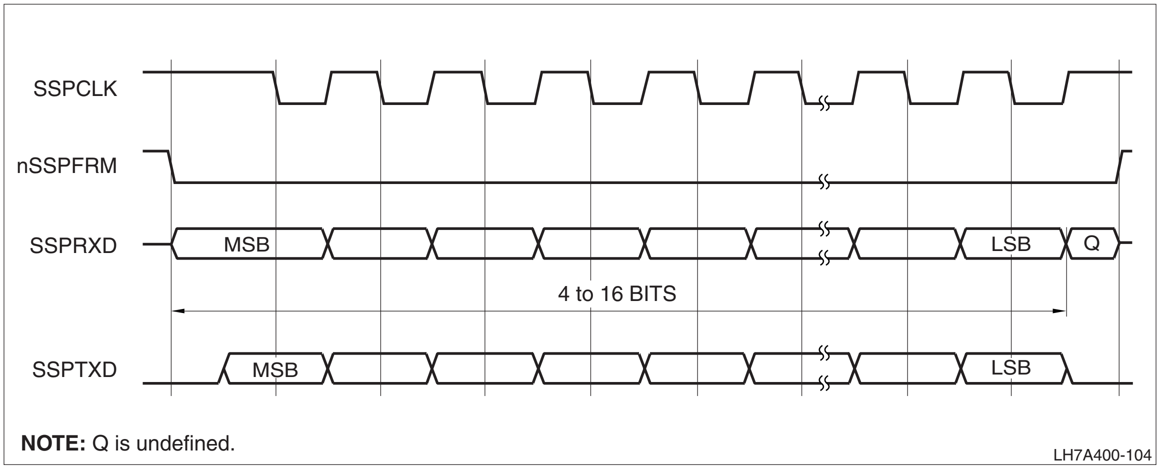


Figure 23. Motorola SPI Frame Format (Single Transfer) with SPO = 1 and SPH = 0

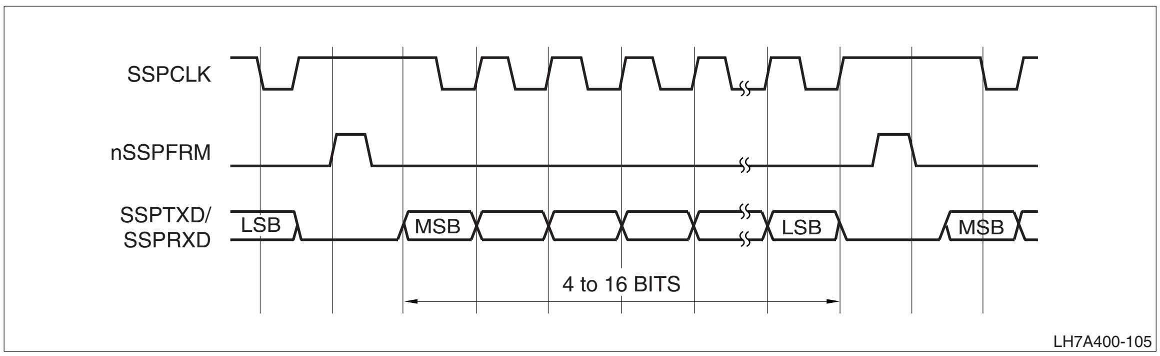


Figure 24. Motorola SPI Frame Format (Continuous Transfer) with SPO = 1 and SPH = 0

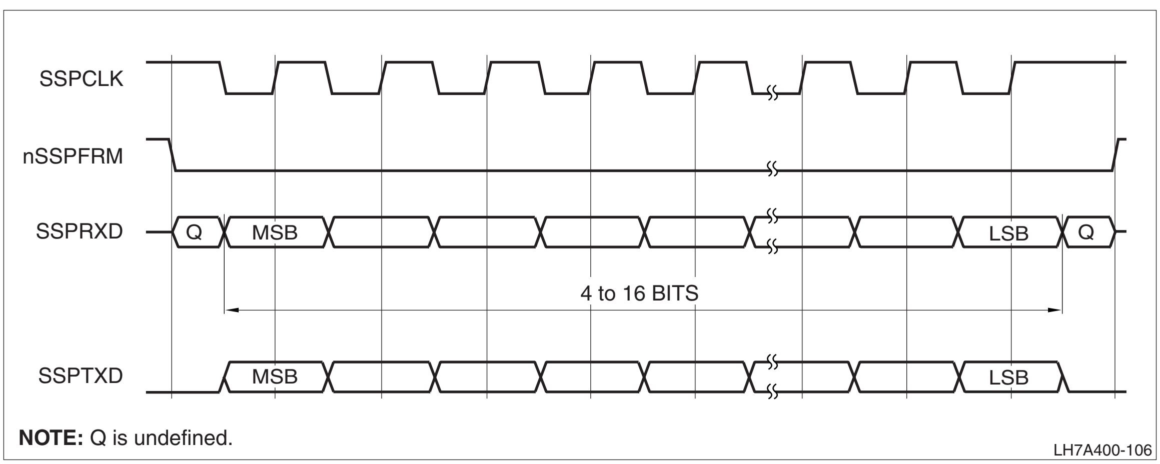


Figure 25. Motorola SPI Frame Format (Single Transfer) with SPO = 1 and SPH = 1

For National Semiconductor MICROWIRE format, the serial frame pin (SSPFRM) is active LOW. Both the SSP and external slave device drive their output data on the falling edge of the clock, and latch data from the other device on the rising edge of the clock. Unlike the full-duplex transmission of the other two frame formats, the National Semiconductor MICROWIRE format utilizes a master-slave messaging technique that operates in half-duplex. When a frame begins in this mode, an 8-bit control message is transmitted to the off-chip slave. During this transmission no incoming data is received by the SSP. After the message has been sent, the external slave device decodes the message. After waiting one serial clock period after the last bit of the 8-bit control message was received it responds by returning the requested data. The returned data can be 4 to 16 bits in length, making the total frame length between 13 to 25 bits. See Figure 26 and Figure 27.

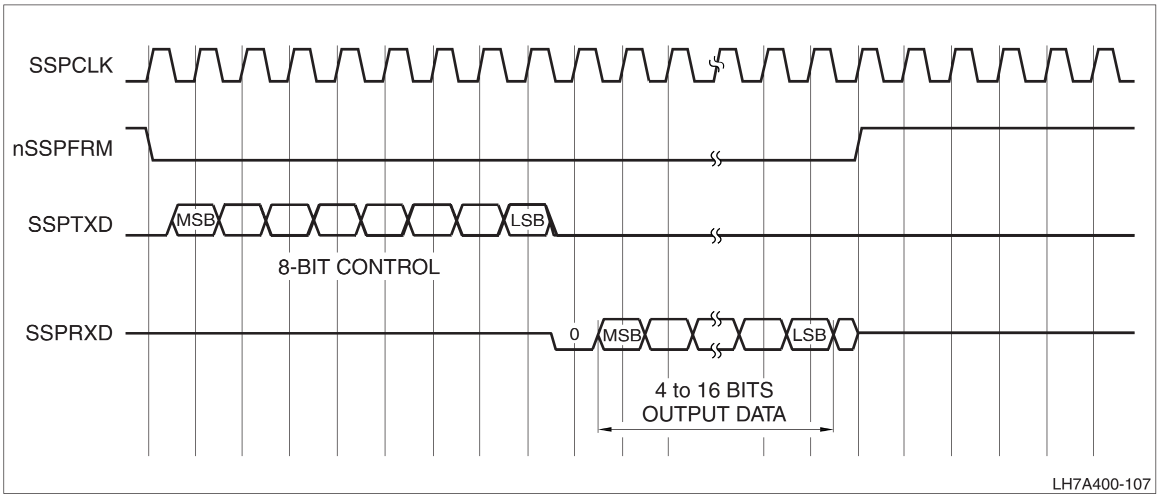


Figure 26. MICROWIRE Frame Format (Single Transfer)

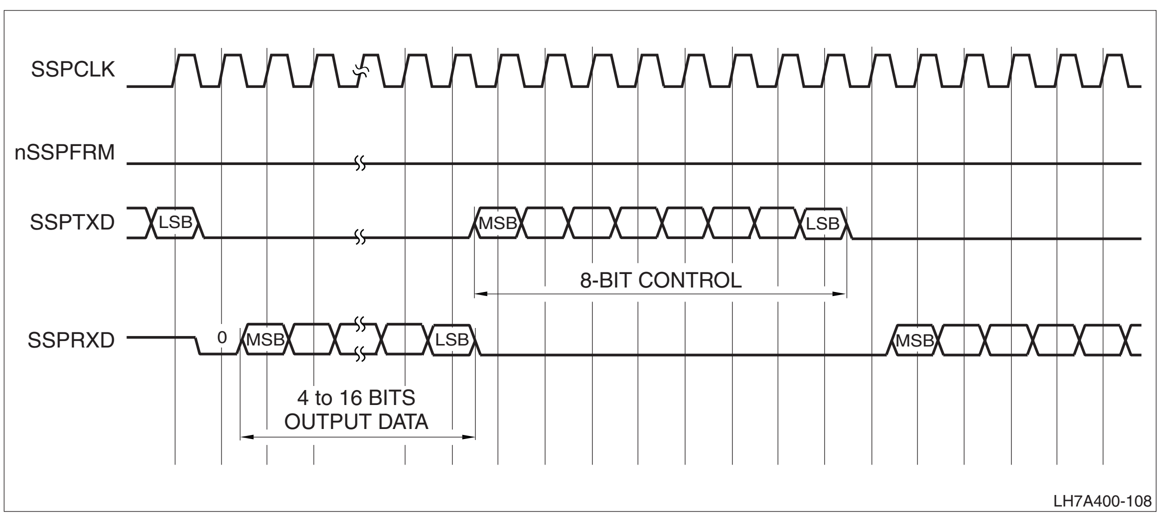
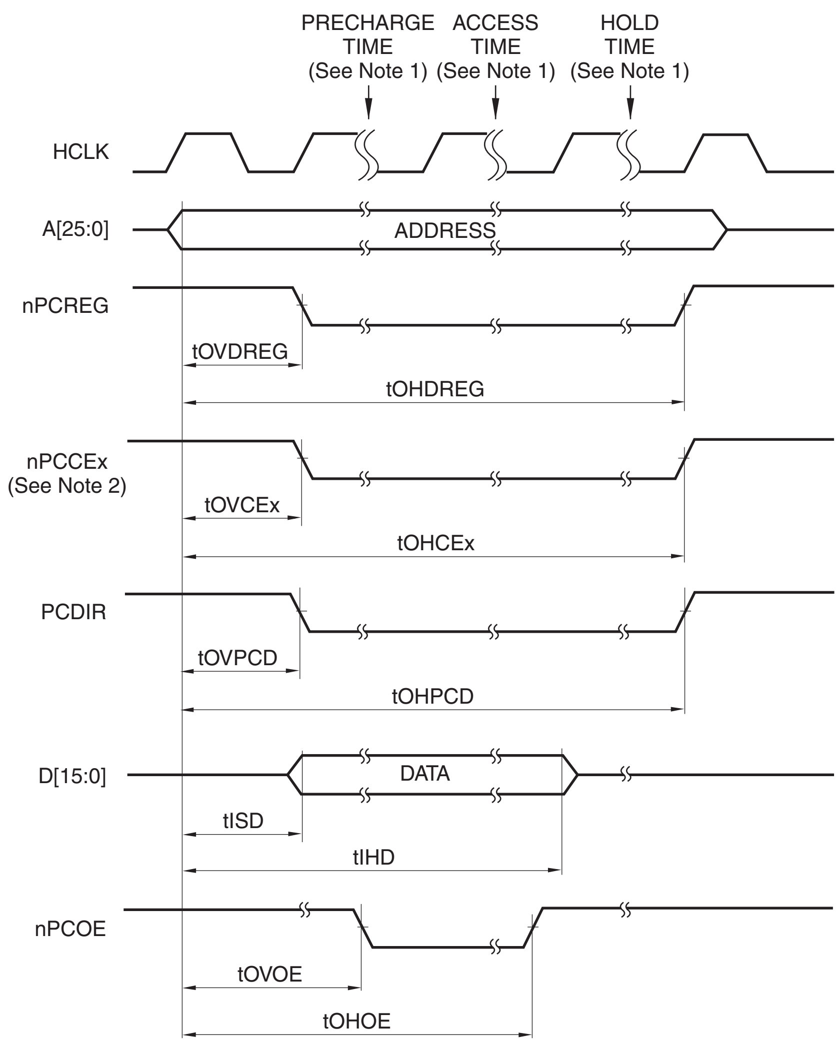


Figure 27. MICROWIRE Frame Format (Continuous Transfers)

PC Card (PCMCIA) Waveforms

Figure 28 shows the waveforms and timing for a PCMCIA Read Transfer, Figure 29 shows the waveforms and timing for a PCMCIA Write Transfer.



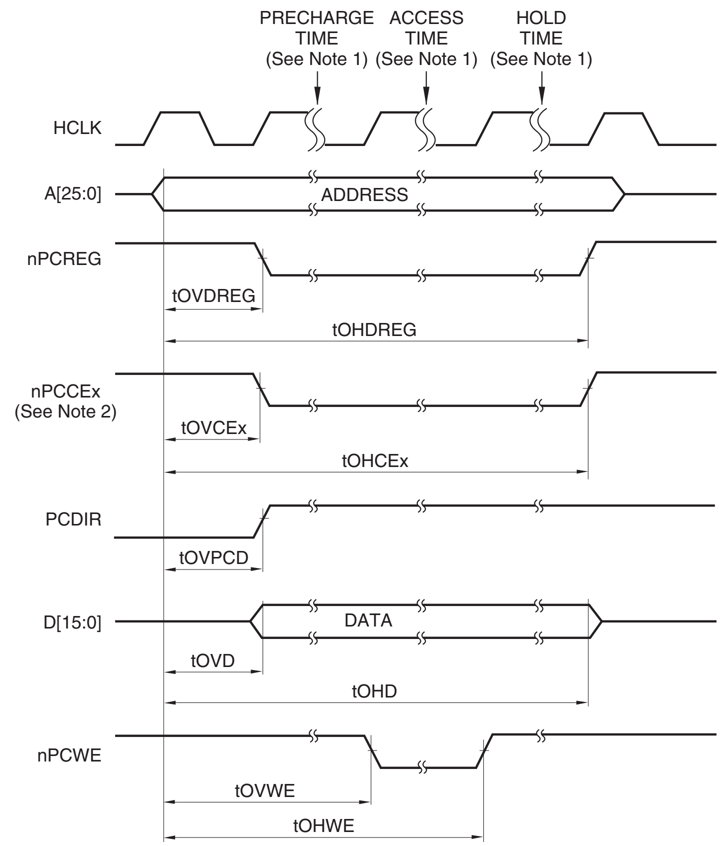
NOTES:

1. Precharge time, access time, and hold time are programmable wait-state times.
2.

nPCCE1	nPCCE2	TRANSFER TYPE
0	0	Common Memory
0	1	Attribute Memory
1	0	I/O
1	1	None

LH7A400-11

Figure 28. PCMCIA Read Transfer



NOTES:

1. Precharge time, access time, and hold time are programmable wait-state times.
2.

nPCCE1	nPCCE2	TRANSFER TYPE
0	0	Common Memory
0	1	Attribute Memory
1	0	I/O
1	1	None

LH7A400-12

Figure 29. PCMCIA Write Transfer

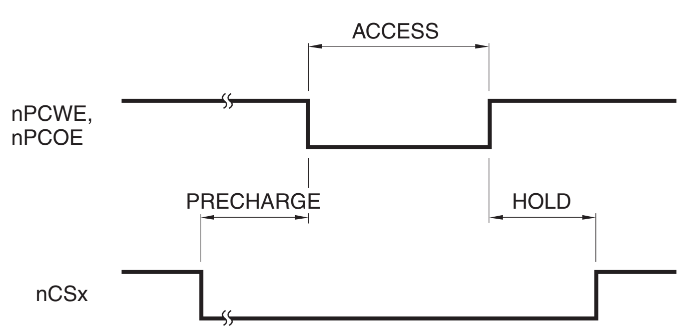


Figure 30. PCMCIA Precharge, Access, and Hold Waveform

MMC Interface Waveform

Figure 31 shows the waveforms and timing for an MMC command or data Read and Write.

AC97 Interface Waveform

Figure 32 shows the waveforms and timing for the AC97 interface Data Setup and Hold.

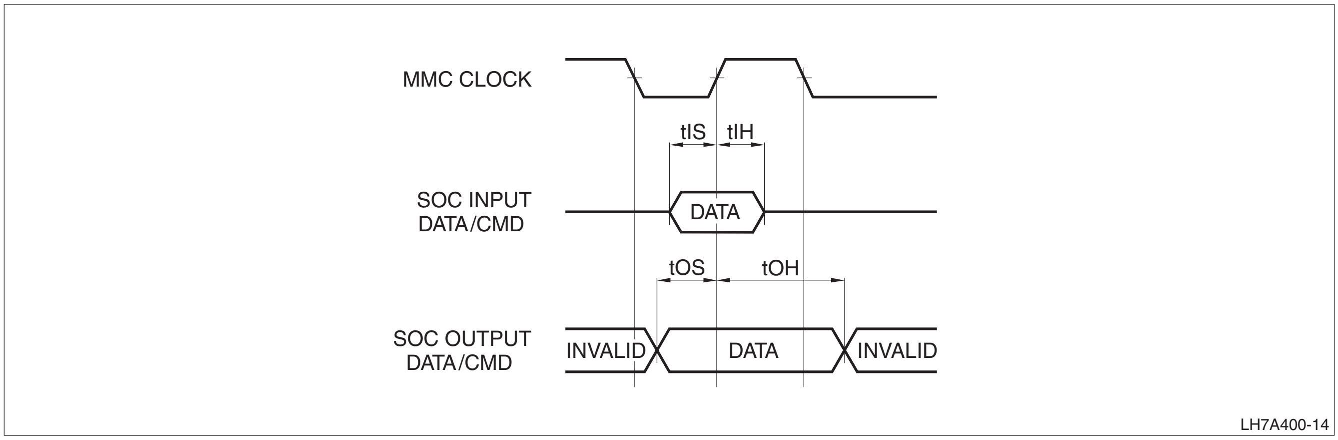


Figure 31. MMC Command/Data Read and Write Timing

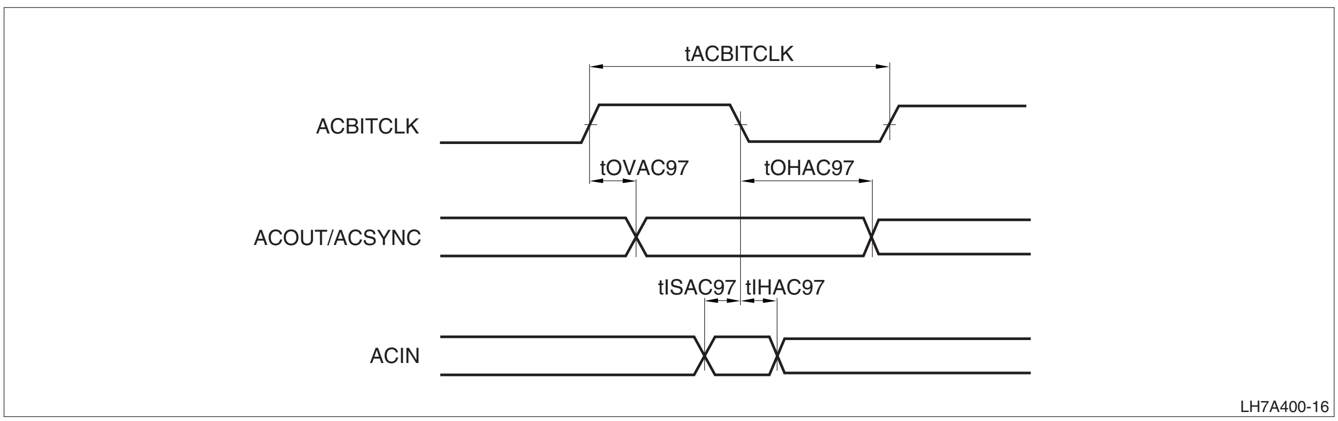


Figure 32. AC97 Data Setup and Hold

Audio Codec Interface Waveforms

Figure 33 and Figure 34 show the timing for the ACI. Transmit data is clocked on the rising edge of ACBITCLK (whether transmitted by the LH7A400 ACI or by the external codec chip); receive data is clocked on the falling edge. This allows full-speed, full duplex operation.

Color LCD Controller Waveforms

Figure 35 shows the Valid Output Setup Time for LCD data. Timing diagrams for each CLCDC mode appear in Figure 36 through Figure 41.

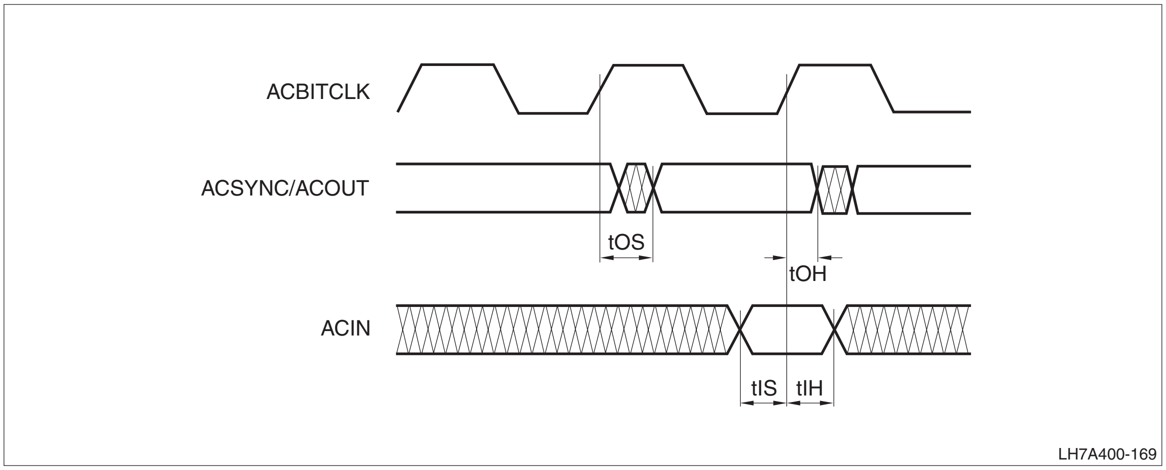


Figure 33. ACI Signal Timing

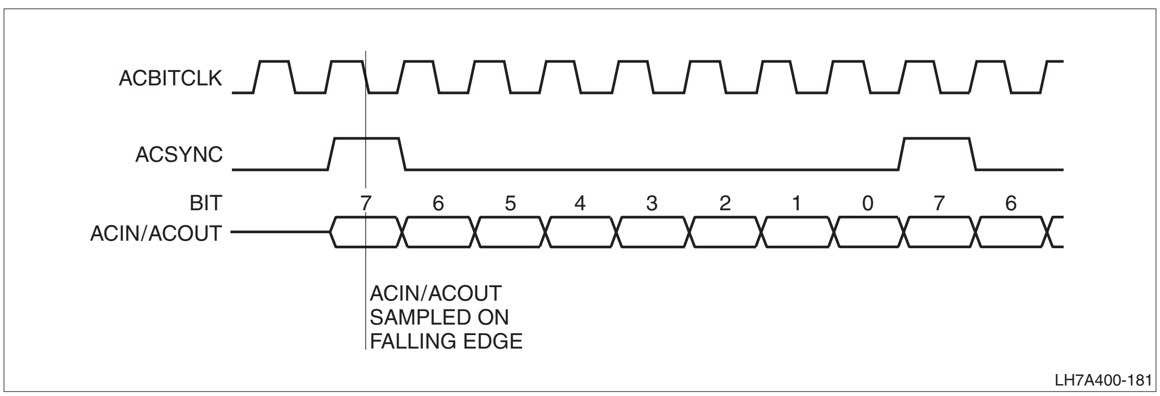


Figure 34. ACI Data stream

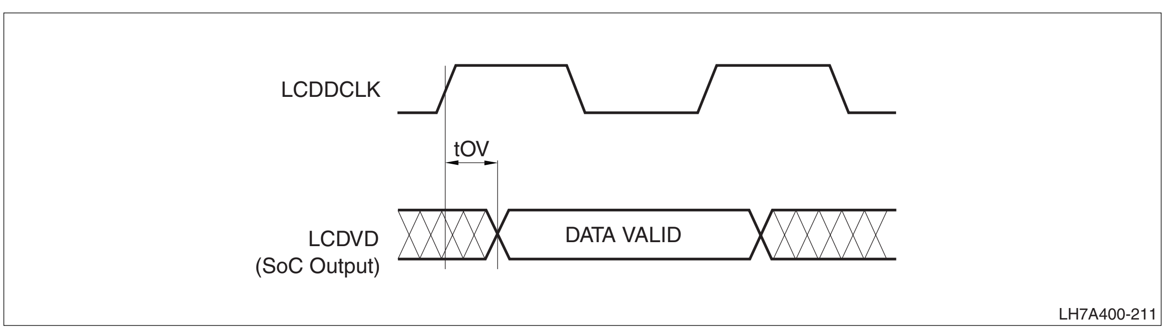


Figure 35. CLCDC Valid Output Data Time

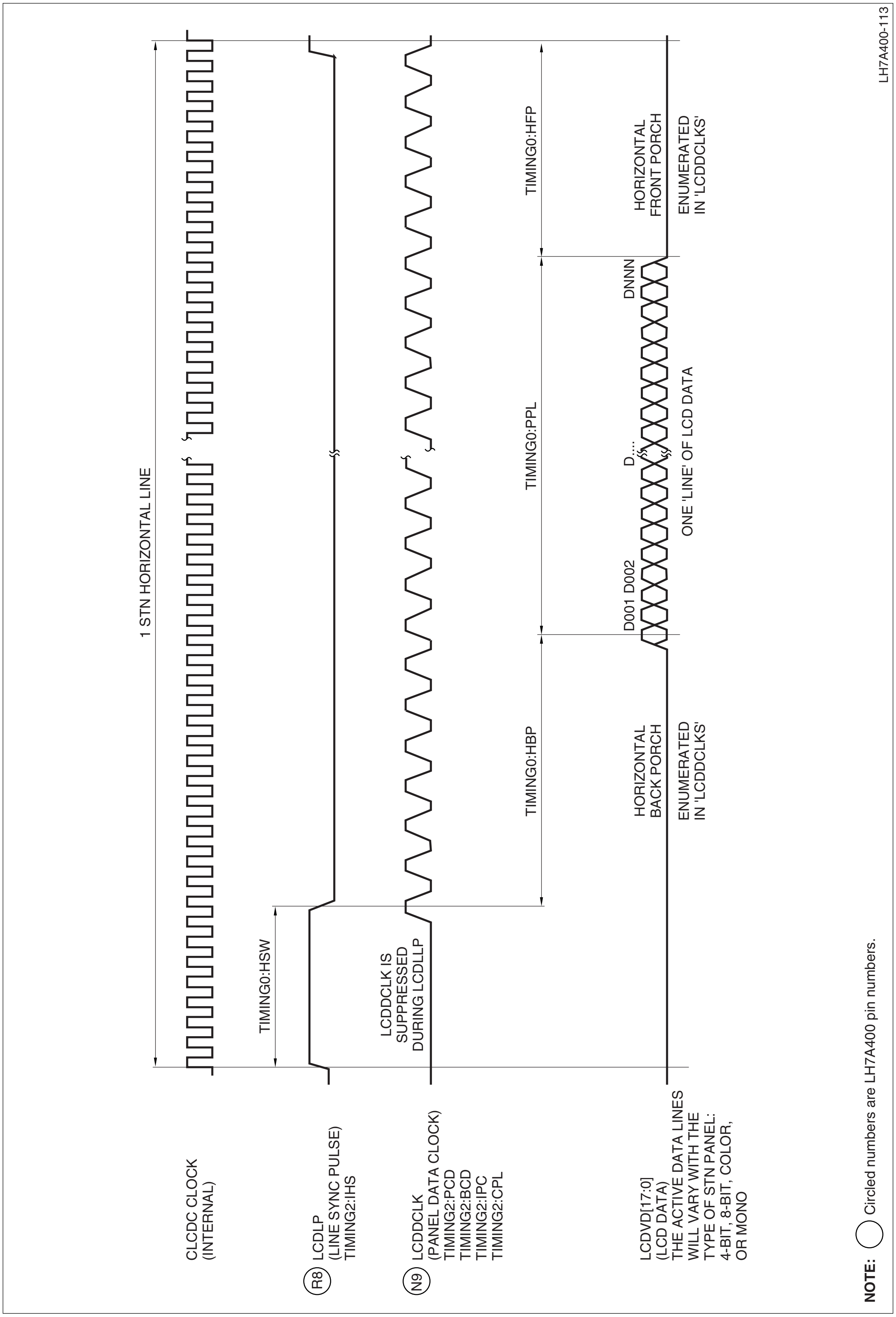


Figure 36. STN Horizontal Timing Diagram

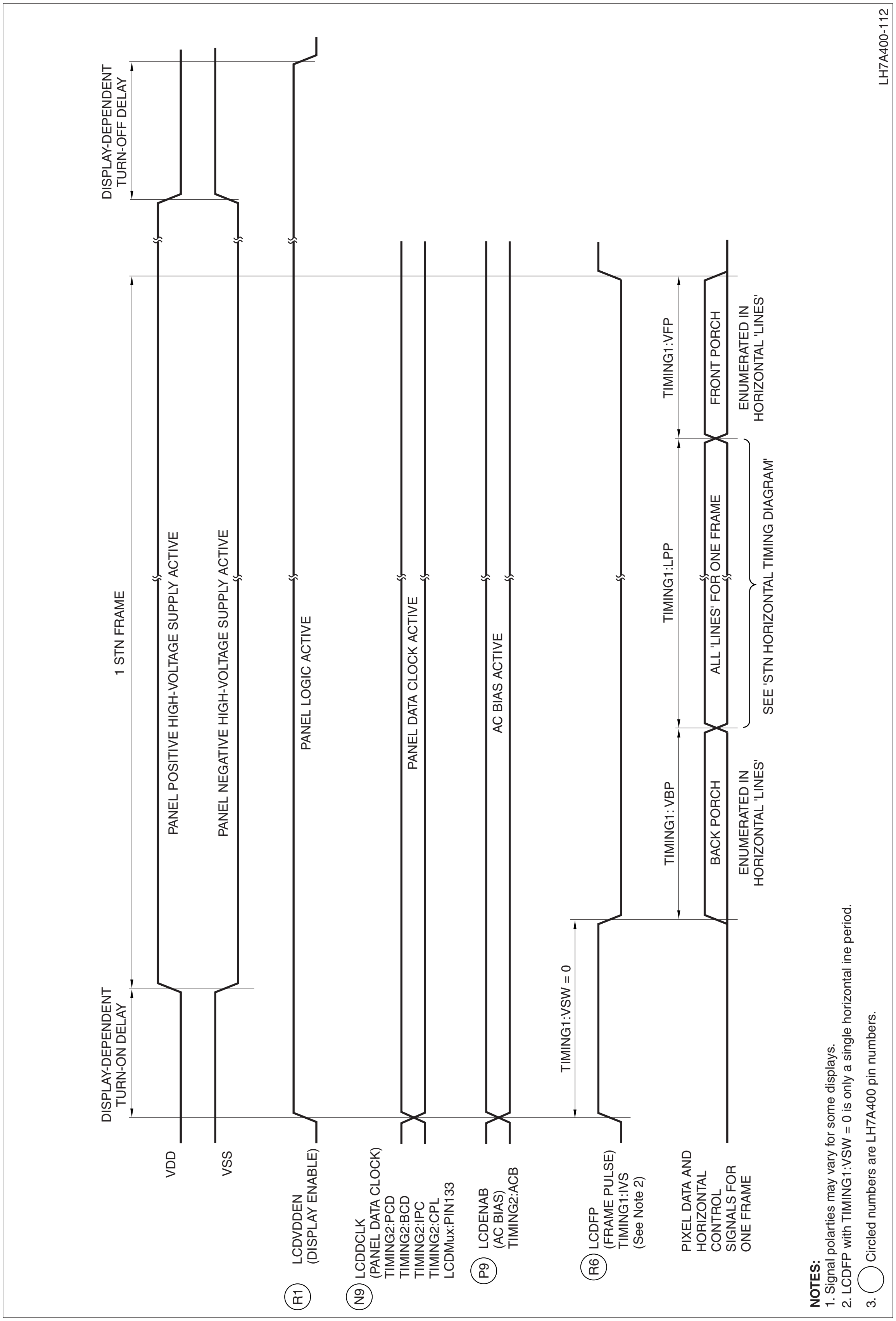


Figure 37. STN Vertical Timing Diagram

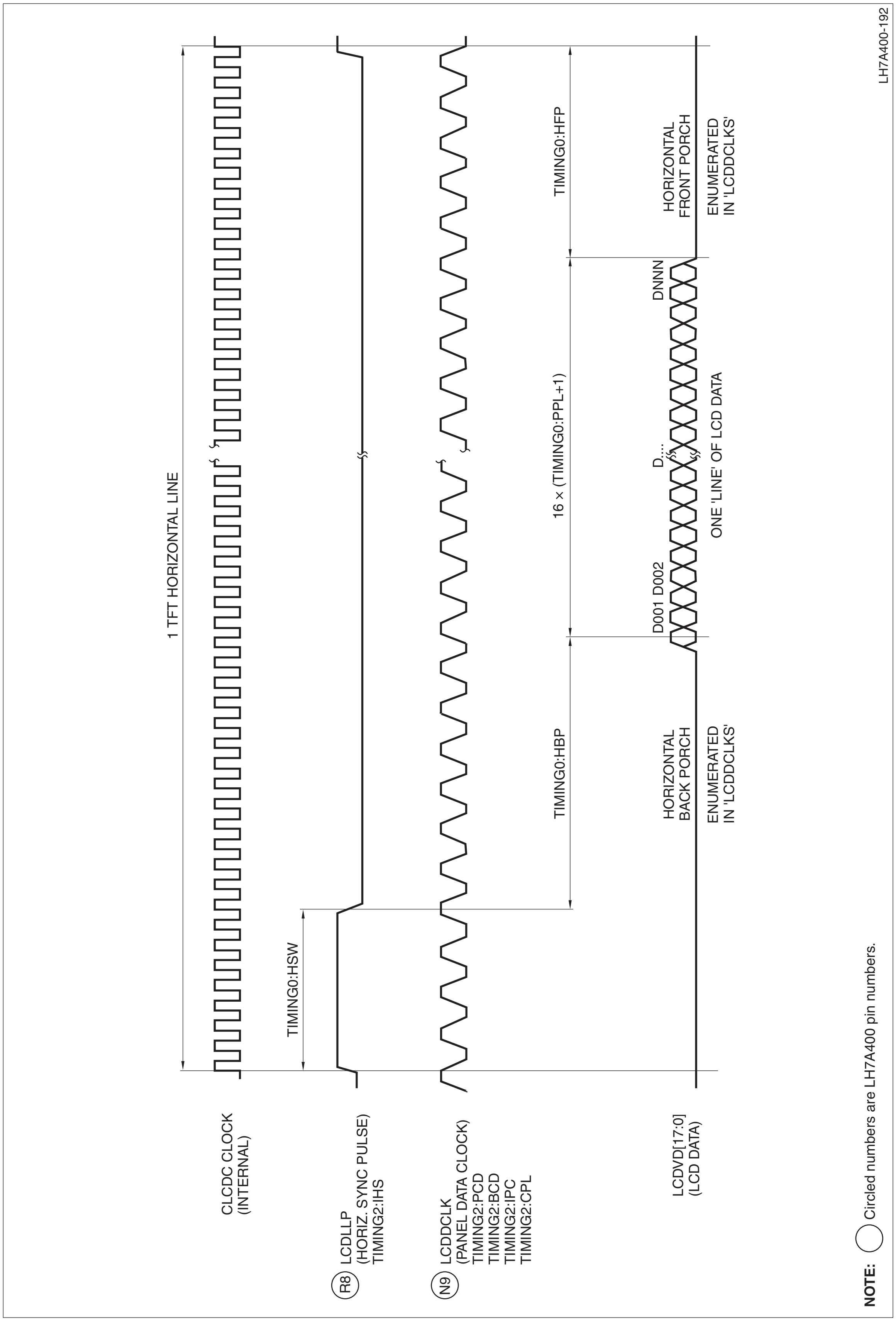


Figure 38. TFT Horizontal Timing Diagram

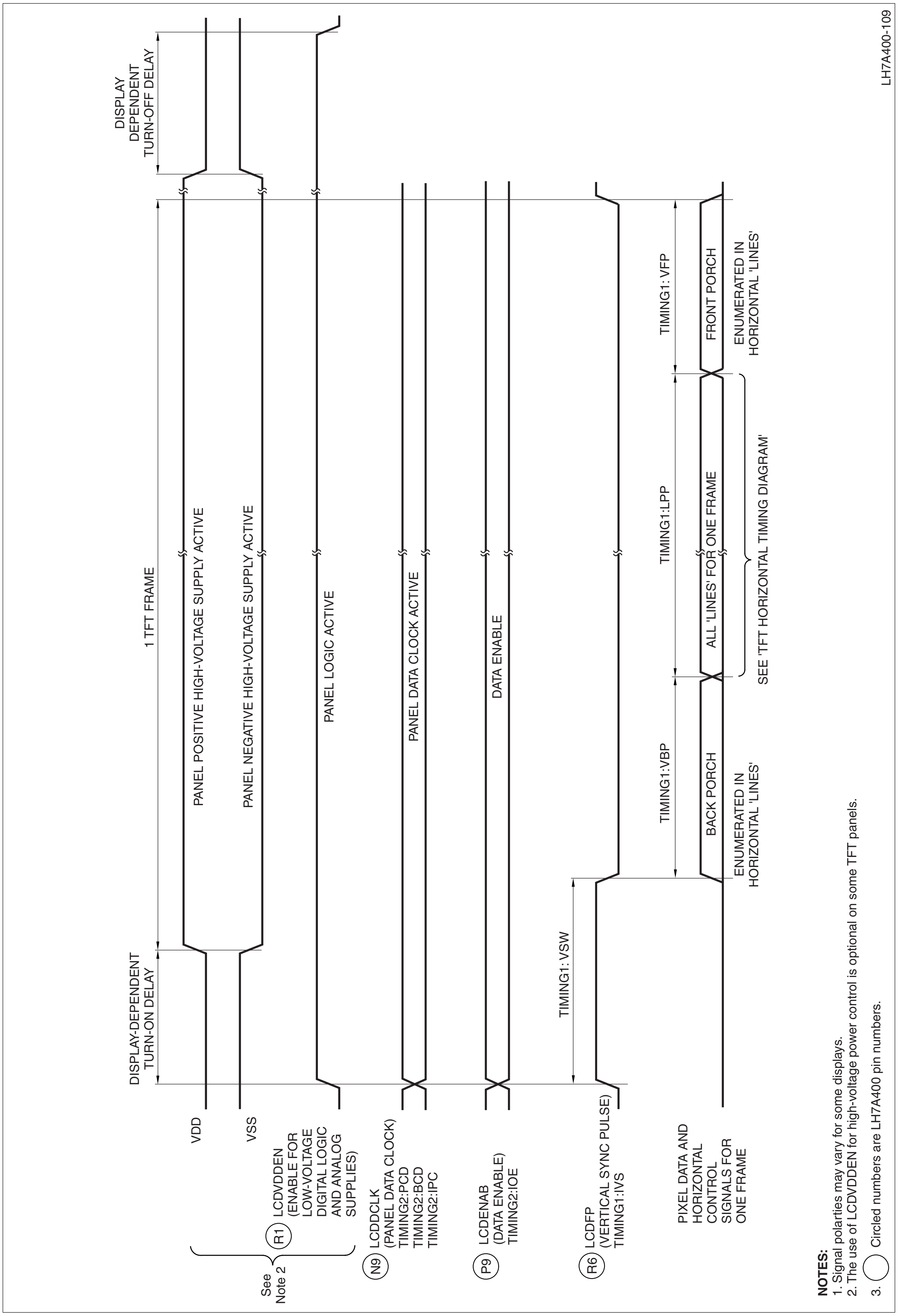


Figure 39. TFT Vertical Timing Diagram

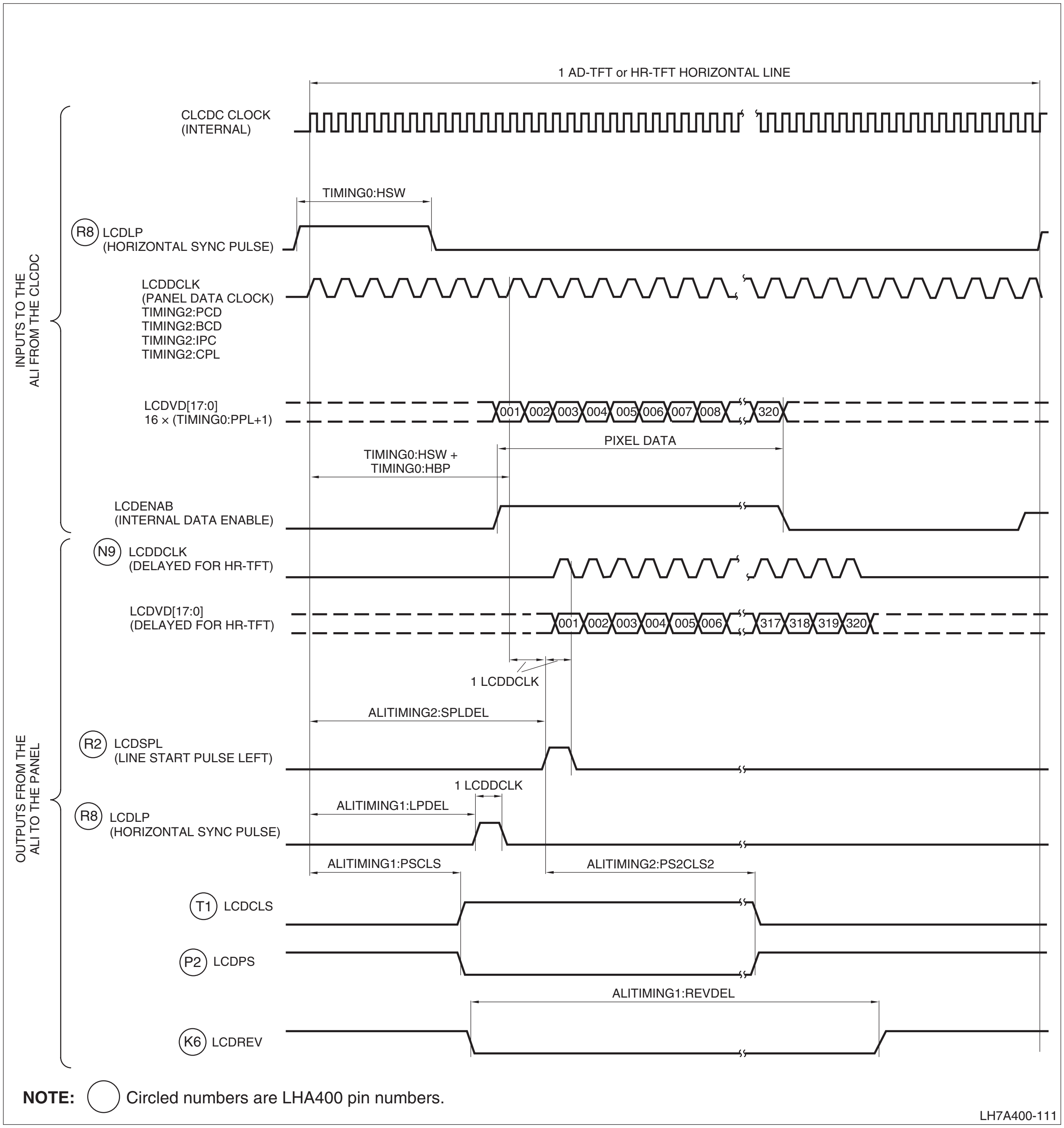


Figure 40. AD-TFT and HR-TFT Horizontal Timing Diagram

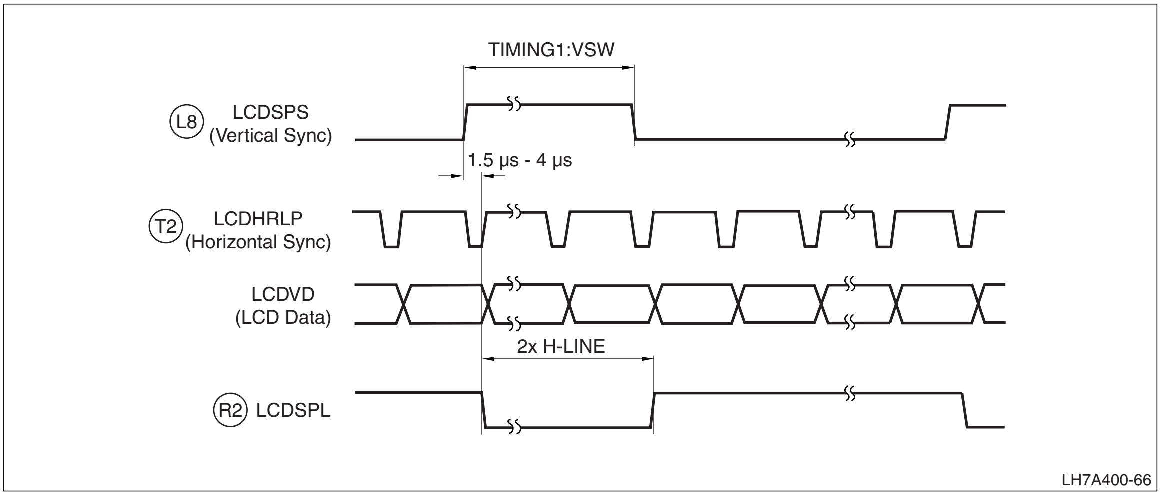


Figure 41. AD-TFT and HR-TFT Vertical Timing Diagram

CLOCK AND STATE CONTROLLER (CSC) WAVEFORMS

Figure 42 shows the behavior of the LH7A400 when coming out of Reset or Power On. Figure 43 shows external reset timing, and Table 13 gives the timing parameters. Figure 44 depicts signal timing following a Reset.

At Power-On, nPOR must be held LOW at least until the 32.768 kHz oscillator is stable, and must be deasserted at least two 32.768 kHz clock periods before the WAKEUP signal is asserted. Once the 14.7456 MHz oscillator is stable, the PLLs require 250 µs to lock.

On transition from Standby to Run (including a Cold Boot), the Wakeup pin must not be asserted for 2 seconds after assertion of nPOR to allow time for sampling BATOK and nEXTPWR. The delay prevents a false 'battery good' indication caused by alkaline battery recovery that can immediately follow a battery-low switch off. The battery sampling takes place on the rising edge of the 1 Hz clock. This clock is derived from the 32.768 kHz oscillator. The WAKEUP pin can be pulsed, but at least one edge must follow the 2 second delay to be recognized. For more information, see the application note "Implementing Auto-Wakeup on the LH7A4xx Series Devices" at www.nxp.com.

Figure 45 shows the recommended components for the NXP LH7A400 32.768 kHz external oscillator circuit. Figure 46 shows the same for the 14.7456 MHz external oscillator circuit. In both figures, the NAND gate represents the internal logic of the chip.

Table 13. Reset AC Timing

PARAMETER	DESCRIPTION	MIN.	MAX.	UNIT
tOSC32	32.768 kHz Oscillator Stabilization Time after Power On*		550	ms
tOSC14	14.7456 MHz Oscillator Stabilization Time after Wake UP		4	ms
tURESET/tPWRFL	nURESET/nPWRFL Pulse Width	4		32.768 kHz clock periods

NOTE: *VDDC = VDDCmin

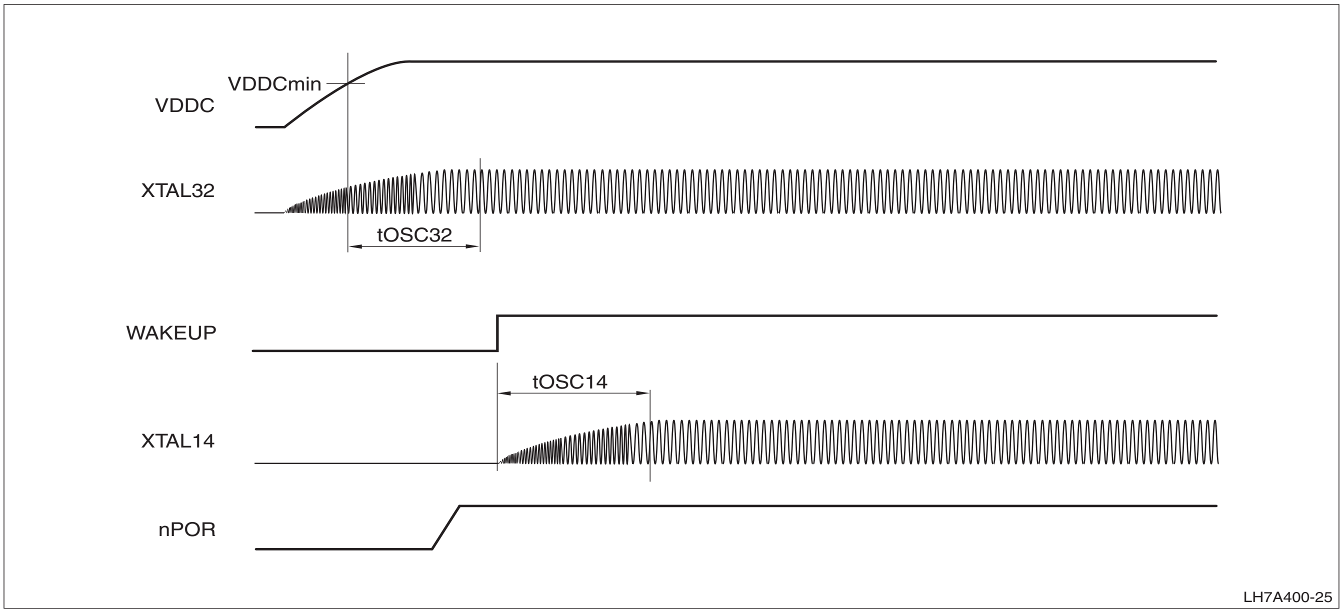


Figure 42. Oscillator Start-up

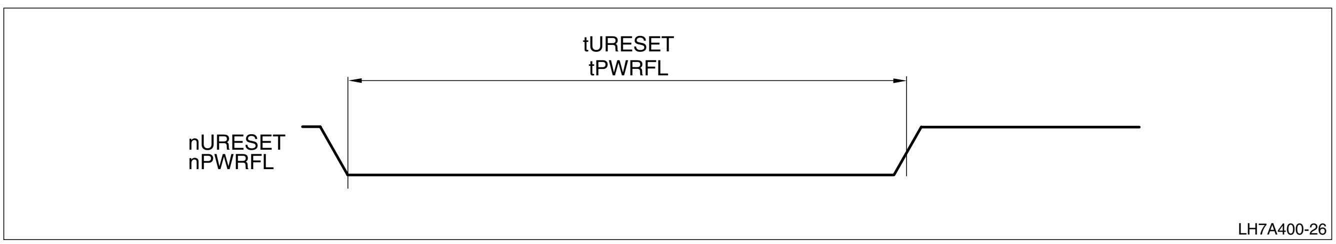


Figure 43. External Reset

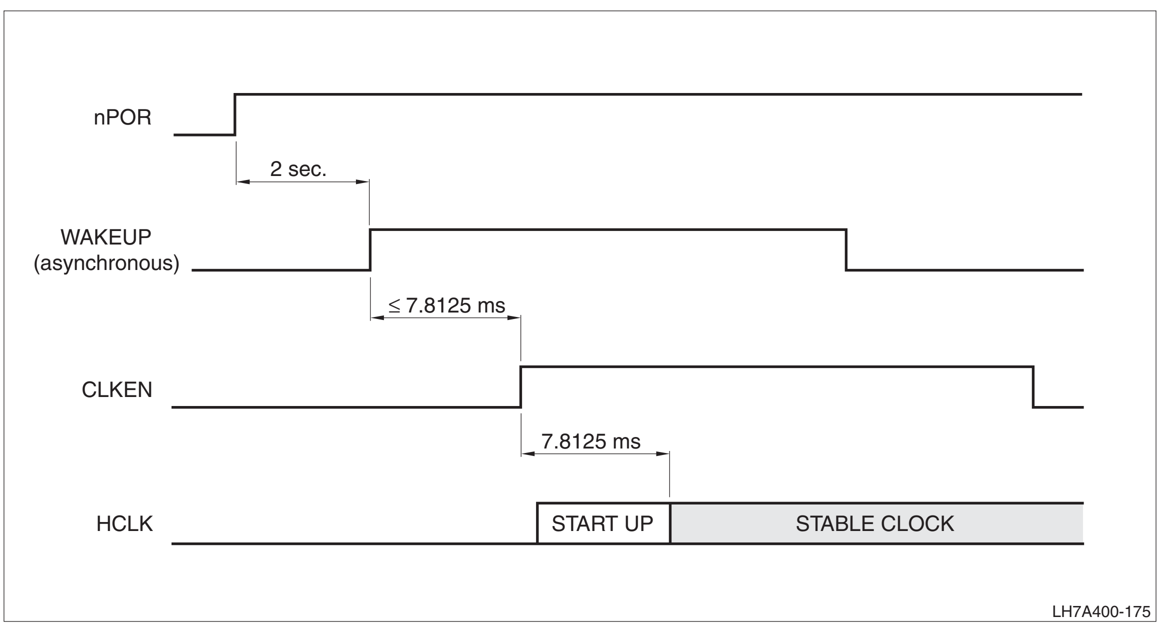
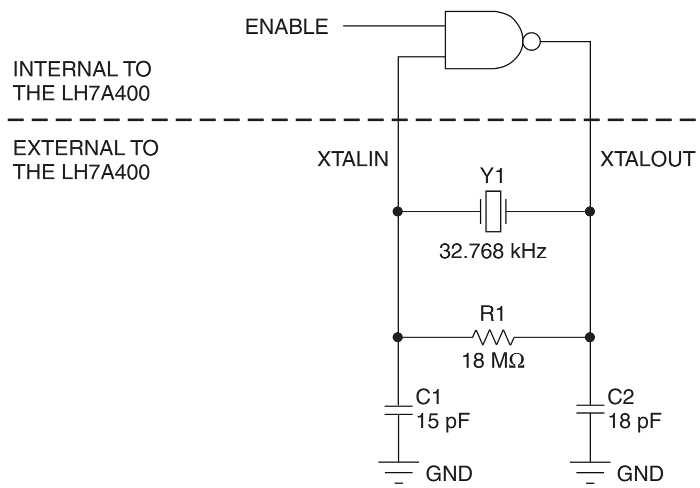


Figure 44. Signal Timing After Reset



NOTES:
1. Y1 is a parallel-resonant type crystal. (See table)
2. The nominal values for C1 and C2 shown are for a crystal specified at 12.5 pF load capacitance (CL).
3. The values for C1 and C2 are dependent upon the cystal's specified load capacitance and PCB stray capacitance.
4. R1 must be in the circuit.
5. Ground connections should be short and return to the ground plane which is connected to the processor's core ground pins.
6. Tolerance for R1, C1, C2 is ≤ 5%.

RECOMMENDED CRYSTAL SPECIFICATIONS

PARAMETER	DESCRIPTION
32.768 kHz Crystal	Parallel Mode
Tolerance	±30 ppm
Aging	±3 ppm
Load Capacitance	12.5 pF
ESR (MAX.)	50 kΩ
Drive Level	1.0 μW (MAX.)
Recommended Part	MTRON SX1555 or equivalent

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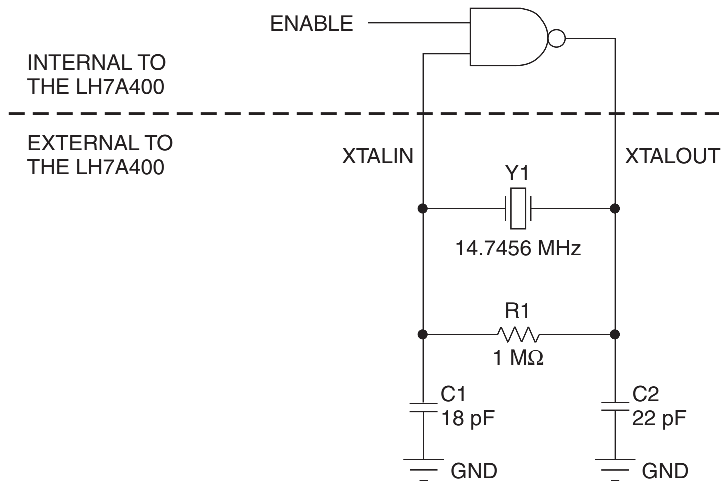
Figure 45. 32.768 kHz External Oscillator Components and Schematic



RECOMMENDED CRYSTAL SPECIFICATIONS

PARAMETER	DESCRIPTION
14.7456 MHz Crystal	(AT-Cut) Parallel Mode
Tolerance	±50 ppm
Stability	±100 ppm
Aging	±5 ppm
Load Capacitance	18 pF
ESR (MAX.)	40 Ω
Drive Level	100 μW (MAX.)
Recommended Part	MTRON SX2050 or equivalent

NOTES:
1. Y1 is a parallel-resonant type crystal. (See table)
2. The nominal values for C1 and C2 shown are for a crystal specified at 18 pF load capacitance (CL).
3. The values for C1 and C2 are dependent upon the cystal's specified load capacitance and PCB stray capacitance.
4. R1 must be in the circuit.
5. Ground connections should be short and return to the ground plane which is connected to the processor's core ground pins.
6. Tolerance for R1, C1, C2 is ≤ 5%.

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Figure 46. 14.7456 MHz External Oscillator Components and Schematic

Operating Temperature and Noise Immunity

The junction temperature, Tj, is the operating temperature of the transistors in the integrated circuit. The switching speed of the CMOS circuitry within the SoC depends partly on Tj, and the lower the operating temperature, the faster the CMOS circuits will switch. Increased switching noise generated by faster switching circuits could affect the overall system stability. The amount of switching noise is directly affected by the application executed on the SoC.

NXP recommends that users implementing a system to meet industrial temperature standards should use an external oscillator rather than a crystal to drive the system clock input of the System-on-Chip. This change from crystal to oscillator will increase the robustness (i.e., noise immunity of the clock input to the SoC).

Printed Circuit Board Layout Practices

LH7A400 POWER SUPPLY DECOUPLING

The LH7A400 has separate power and ground pins for different internal circuitry sections. The VDD and VSS pins supply power to I/O buffers, while VDDC and VSSC supply power to the core logic, and VDDA/VSSA supply analog power to the PLLs.

Each of the VDD and VDDC pins must be provided with a low impedance path to the corresponding board power supply. Likewise, the VSS, VSSA, and VSSC pins must be provided with a low impedance path to the board ground.

Each power supply must be decoupled to ground using at least one 0.1 μF high frequency capacitor located as close as possible to a VDDx, VSSx pin pair on each of the four sides of the chip. If room on the circuit board allows, add one 0.01 μF high frequency capacitor near each VDDx, VSSx pair on the chip.

To be effective, the capacitor leads and associated circuit board traces connecting to the chip VDDx, VSSx pins must be kept to less than half an inch (12.7 mm) per capacitor lead. There must be one bulk 10 μF capacitor for each power supply placed near one side of the chip.

RECOMMENDED PLL, VDDA, VSSA FILTER

The VDDA pins supply power to the chip PLL circuitry. VSSA is the ground return path for the PLL circuit. NXP recommends a low-pass filter attached as shown in Figure 47. The values of the inductor and capacitors are not critical. The low-pass filter prevents high frequency noise from adversely affecting the PLL circuits. The distance from the IC pin to the high frequency capacitor should be as short as possible.

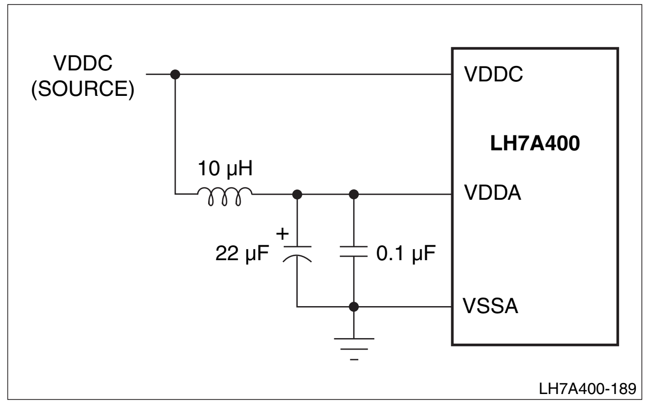


Figure 47. VDDA, VSSA Filter Circuit

UNUSED INPUT SIGNAL CONDITIONING

Floating input signals can cause excessive power consumption. Unused inputs without internal pull-up or pull-down resistors should be pulled up or down externally (NXP recommends tying HIGH), to tie the signal to its inactive state. 33 KΩ or less is recommended.

Some GPIO signals default to inputs. If the pins that carry these signals are unused, software can program these signals as outputs, eliminating the need for pull-ups or pull-downs. Power consumption may be higher than expected until software completes programming the GPIO. Some LH7A400 inputs have internal pull-ups or pull-downs. If unused, these inputs do not require external conditioning.

OTHER CIRCUIT BOARD LAYOUT PRACTICES

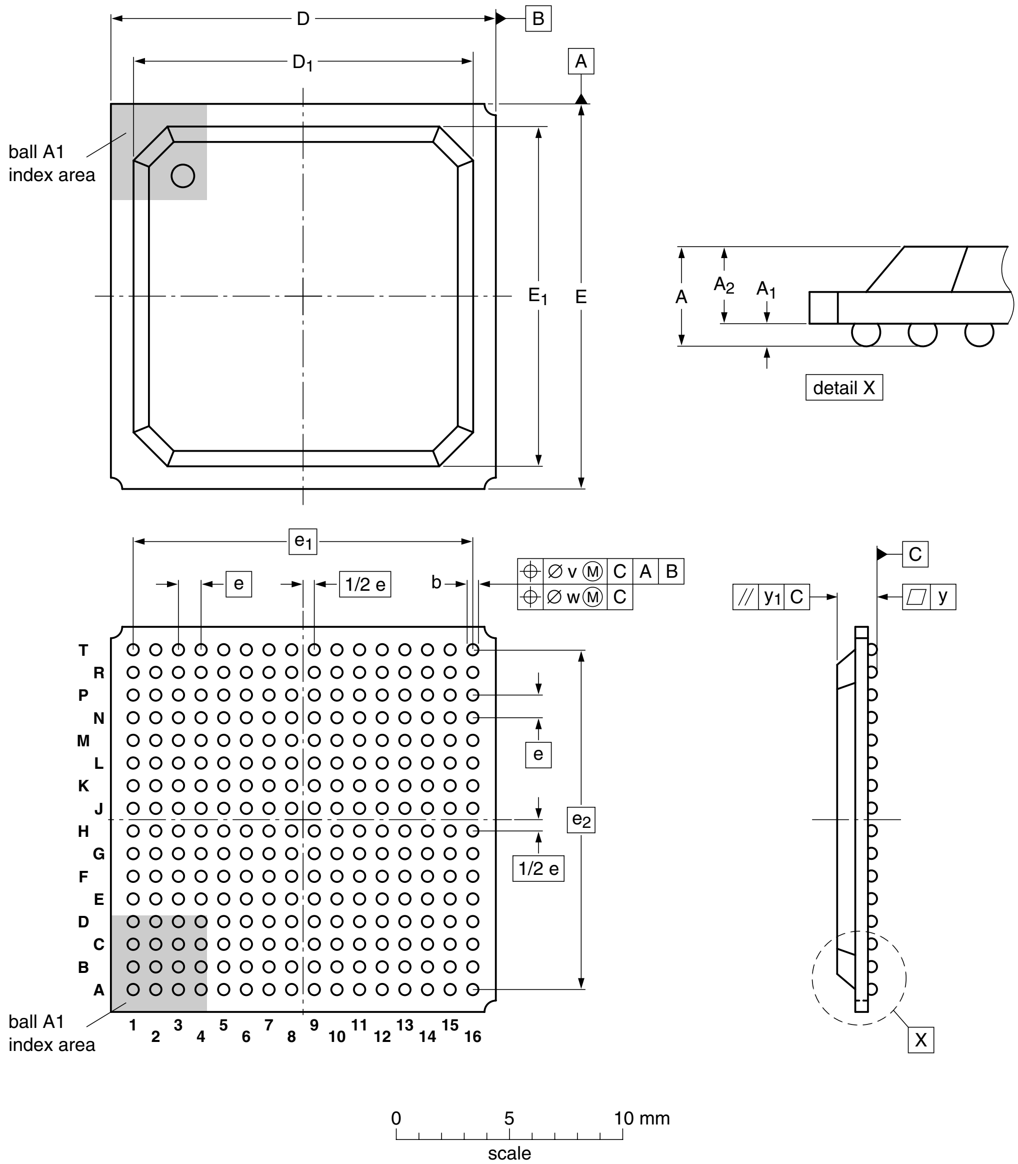
All outputs have fast rise and fall times. Printed circuit trace interconnection length must therefore be reduced to minimize overshoot, undershoot and reflections caused by transmission line effects of these fast output switching times. This recommendation particularly applies to the address and data buses.

When considering capacitance, calculations must consider all device loads and capacitances due to the circuit board traces. Capacitance due to the traces will depend upon a number of factors, including the trace width, dielectric material the circuit board is made from and proximity to ground and power planes.

Attention to power supply decoupling and printed circuit board layout becomes more critical in systems with higher capacitive loads. As these capacitive loads increase, transient currents in the power supply and ground return paths also increase.

PACKAGE SPECIFICATIONS

BGA256: plastic ball grid array package; 256 balls **SOT1018-1**



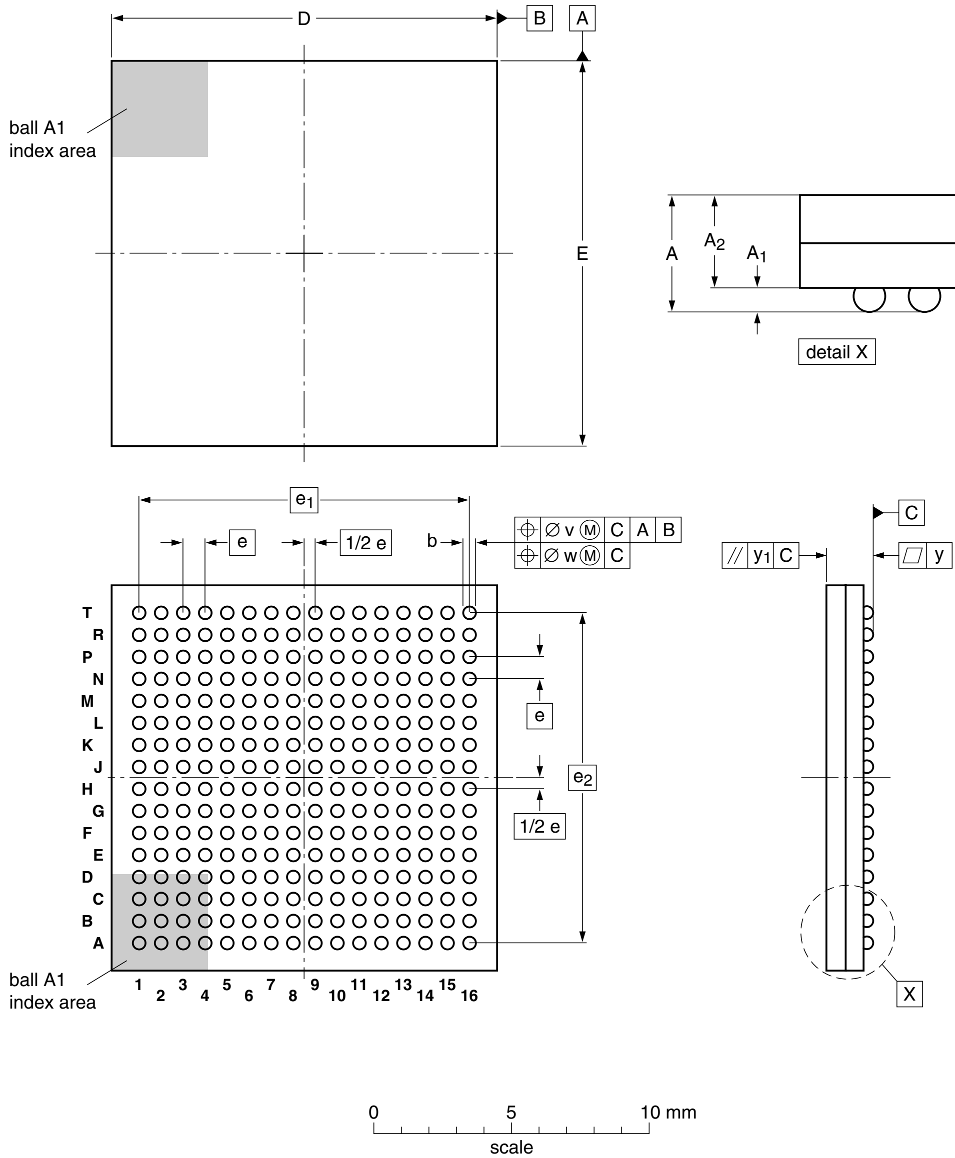
DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	D_1	E	E_1	e	e_1	e_2	v	w	y	y_1
mm	1.95	0.5 0.3	1.45 1.25	0.55 0.45	17.2 16.8	15.75 14.75	17.2 16.8	15.75 14.75	1	15	15	0.25	0.1	0.15	0.35

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1018-1						

Figure 48. Package outline SOT1018-1 (BGA256)

LFBGA256: plastic low profile fine-pitch ball grid array package; 256 balls **SOT1020-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.7	0.4 0.3	1.35 1.15	0.5 0.4	14.1 13.9	14.1 13.9	0.8	12	12	0.15	0.08	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1020-1						

Figure 49. Package outline SOT1020-1 (LFBGA256)

REVISION HISTORY

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LH7A400_N_1	20070716	Preliminary data sheet	-	FAST LH7A400 v1-5 5-9-07
Modifications: • First NXP version based on the LH7A400 data sheet of 20070509				

1. Legal information

1.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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