# PI6CL10804

## 1.2V/1.5V, 200MHz, 1:4 Networking Clock Buffer

### Features

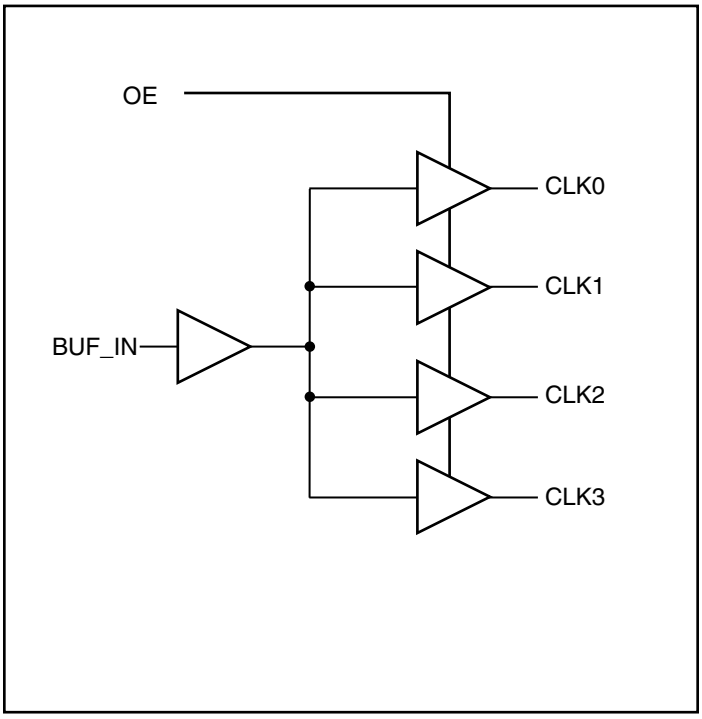
- High-speed, low-noise, non-inverting 1:4 buffer
- Maximum Frequency up to 200 MHz
- Low output skew < 100ps
- Low propagation delay < 3.5ns
- Optimized duty cycle
- 1.2V or 1.5V supply voltage
- Packages (Pb-free & Green available):
  -8-pin SOIC (W)

### Description

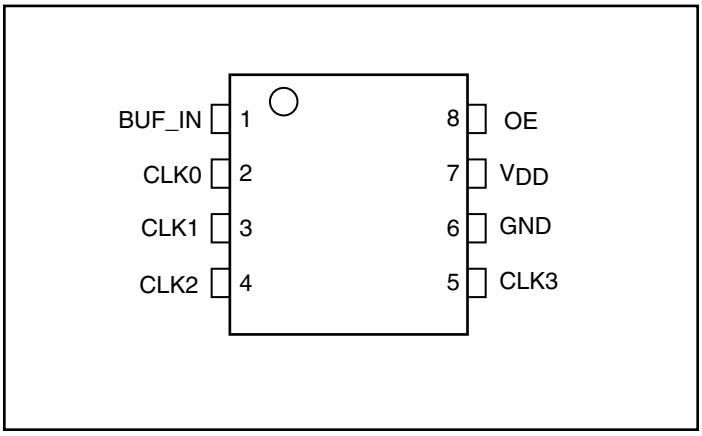
The PI6CL10804 is a 1.2V or 1.5V high-speed, low-noise 1:4 non-inverting clock buffer. The key goal in designing the PI6CL10804 is to target networking applications that require low-skew, low-jitter, and high-frequency clock distribution.

Providing output-to-output skew as low as 100ps, the PI6CL10804 is an ideal clock distribution device for synchronous systems. Designing synchronous networking systems requires a tight level of skew from a large number of outputs.

### Block Diagram




### Pin Configuration




### Pin Description

| Pin Name | Description |
|---|---|
| BUF_IN | Input |
| CLK [0:3] | Outputs |
| GND | Ground |
| $V_{DD}$ | Power |
| OE | Output Enable |

## 1.5V Absolute Maximum Ratings (Above which the useful life may be impaired. For user guidelines only, not tested.)

| | |
|---|---|
| Storage Temperature | –65°C to +150°C |
| $V_{DD}$ Voltage | –0.5V to +2.6V |
| Output Voltage (max. 3.6V) | –0.5V to $V_{DD}$+0.5V |
| Input Voltage (max 3.6V) | –0.5V to $V_{DD}$+0.5V |

**Note:**
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## 1.5V DC Characteristics (Over Operating Range: $V_{DD}$ = 1.5V ± 0.1V, $T_A$ = -40° to 85°C)

| Parameters | Description | Test Conditions(1) | | Min. | Typ.(2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | | 1.4 | 1.5 | 1.6 | V |
| $V_{IH}$ | Input HIGH Voltage | Logic HIGH level | | 0.65 x $V_{DD}$ | | $V_{DD}$ | V |
| $V_{IL}$ | Input LOW Voltage | Logic LOW level | | -0.3 | | 0.35 x $V_{DD}$ | V |
| $I_I$ | Input Current | $V_{DD}$ = Max, Vin = $V_{DD}$ or GND | I pins | | | 15 | µA |
| $V_{OH}$ | Output High Voltage | $V_{DD}$ = Min., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -2mA | 1.05 | | | V |
| | | | $I_{OH}$ = -8mA | 0.75 | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{DD}$ = Min., $V_{IN}$ - $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 1mA | | | 0.4 | V |
| | | | $I_{OL}$ = 2mA | | | 0.35 | |
| | | | $I_{OL}$ = 8mA | | | 0.35 | V |

**Notes:**
1. For Max. or Min. conditions, use appropriate operating range values.
2. Typical values are at $V_{CC}$ = 1.5V, +25°C ambient and maximum loading.

## 1.5V AC Characteristics (Over Operating Range: $V_{DD}$ = 1.5V ± 0.1V, $T_A$ = -40° to 85°C)

| Parameters | Description | Test Conditions(1) | Min. | Typ | Max. | Units |
|---|---|---|---|---|---|---|
| $F_{IN}$ | Input Frequency | | 0 | | 200 | MHz |
| $t_R/t_F$ | CLKn Rise/Fall Time | 20% to 80% | | | 1.5 | ns |
| $t_{PLH}$, $t_{PHL}$(2) | Propagation Delay BUF_IN to CLKn | $C_L$ = 5pF, 125 MHz Outputs are measured @ Vdd/2 | 1.0 | 1.5 | 3.0 | ns |
| $t_{SK(O)}$(3) | Output to Output Skew between any two outputs of the same device @ same transition | | | | 100 | ps |
| $t_{SK(T)}$(3) | Part to Part Skew between two identical outputs of different parts on the same board(4) | | | | 300 | ps |
| $t_{dc\_in}$ | Duty Cycle In @ 1ns edge rate | | 45 | | 55 | % |
| $t_{dc\_out}$ | Duty Cycle Out | | 40 | | 60 | % |

**Notes:**
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew measured at worse cast temperature (max. temp).
4. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.

## 1.2V Absolute Maximum Ratings (Above which the useful life may be impaired. For user guidelines only, not tested.)

| | |
|---|---|
| Storage Temperature | –65°C to +150°C |
| $V_{DD}$ Voltage | –0.5V to +2.5V |
| Output Voltage (max 2.5V) | –0.5V to $V_{DD}$+0.5V |
| Input Voltage (max 2.5V) | –0.5V to $V_{DD}$+0.5V |

**Note:**
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## 1.2V DC Characteristics (Over Operating Range: $V_{DD}$ = 1.2V ± 0.1V, $T_A$ = -40° to 85°C)

| Parameters | Description | Test Conditions(1) | | Min. | Typ.(2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | | 1.1 | 1.2 | 1.3 | V |
| $V_{IH}$ | Input HIGH Voltage | Logic HIGH level | | 0.65*Vdd | | $V_{DD}$ | V |
| $V_{IL}$ | Input LOW Voltage | Logic LOW level | | -0.3 | | 0.35*$V_{DD}$ | |
| $I_I$ | Input Current(3) | $V_{DD}$ = Max, Vin = $V_{DD}$ or GND | I pin | | | 15 | µA |
| $V_{OH}$ | Output High Voltage | $V_{DD}$ = Min., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -2mA | 0.85 | | | V |
| | | | $I_{OH}$ = -8mA | 0.55 | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{DD}$ = Min., $V_{IN}$ - $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 2mA | | | 0.35 | |
| | | | $I_{OL}$ = -8mA | | | 0.45 | |

**Notes:**
1. For Max. or Min. conditions, use appropriate operating Vdd and Ta values.
2. Typical values are at $V_{CC}$ = 1.2V, +25°C ambient and maximum loading.

## 1.2V AC Characteristics (Over Operating Range: $V_{DD}$ = 1.2V ± 0.1V, $T_A$ = -40° to 85°C)

| Parameters | Description | Test Conditions(1) | Min. | Typ | Max. | Units |
|---|---|---|---|---|---|---|
| $F_{IN}$ | Input Frequency | | 0 | | 200 | MHz |
| $t_R/t_F$ | CLKn Rise/Fall Time | 20% to 80% | | | 1.5 | ns |
| $t_{PLH}$, $t_{PHL}$(2) | Propagation Delay BUF_IN to CLKn | $C_L$ = 5pF, 125 MHz Outputs are measured @ Vdd/2 | 1.0 | 2.0 | 3.5 | ns |
| $t_{SK(O)}$(3) | Output to Output Skew between any two outputs of the same device @ same transition | | | | 100 | ps |
| $t_{SK(T)}$(3) | Part to Part Skew between two identical outputs of different parts on the same board(4) | | | | 300 | |
| $t_{dc\_in}$ | Duty Cycle In @ 1ns edge rate | | 45 | | 55 | % |
| $t_{dc\_out}$ | Duty Cycle Out | | 40 | | 60 | |

**Notes:**
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew measured at worse cast temperature (max. temp).
4. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.

## Power Supply Characteristics

| Parameters | Description | Test Conditions[1] | | Min. | Typ. [2] | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_{DDQ}$ | Quiescent Power Supply Current | $V_{DD}$ = 1.5V | $V_{IN}$ = GND or $V_{DD}$ | | | 10 | µA |
| | | $V_{DD}$ = 1.2V | | | | 10 | |
| $I_{DD\_TOT}$ | Total Power Supply Current | $V_{DD}$ = 1.5V | All Outputs Toggling, $C_L$ = 5pF, $F_{IN}$ = 125MHz | | | 15 | mA |
| | | $V_{DD}$ = 1.2V | | | | 10 | |

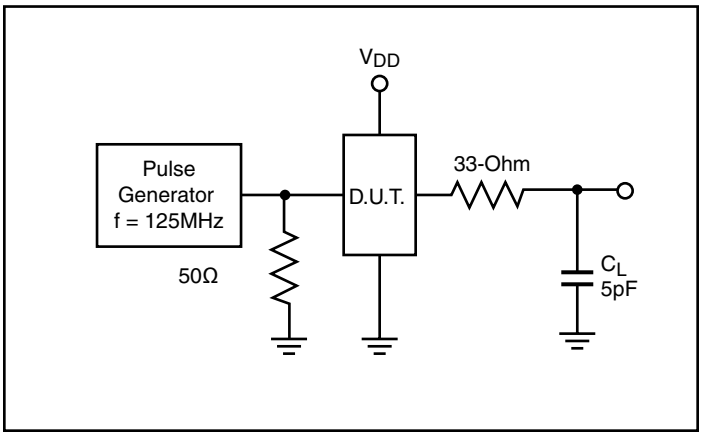
**Notes:**
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics.
2. Typical values are at $V_{CC}$ = 1.2V or 1.5V, and +25°C ambient.

## Capacitance ($T_A$ = 25°C, f = 1 MHz)

| Parameters[1] | Description | Test Conditions | Typ | Max. | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 2.0 | 4 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 1.7 | 6 | |

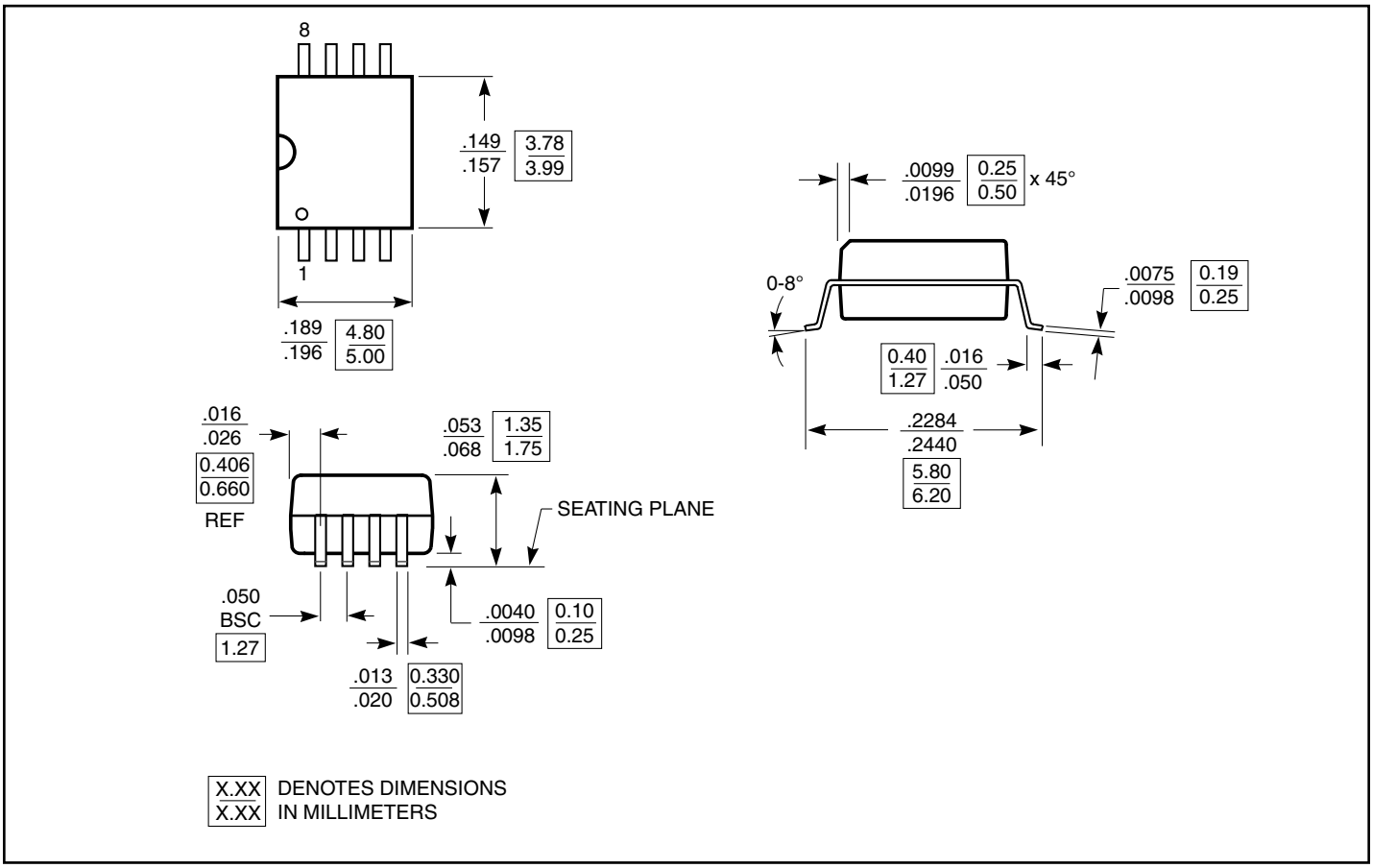
**Note:**
1. This parameter is determined by device characterization but is not production tested.

## Test Circuits for All Outputs




**Definitions:**
$C_L$ = Load capacitance: includes jig and probe capacitance.

## Packaging Mechanical: 8-Pin SOIC (W)



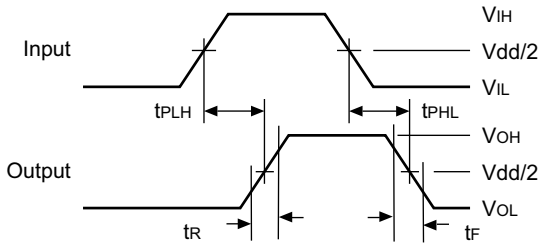

## Ordering Information[1,2,3]

| Ordering Code | Package Code | Package Type |
|---|---|---|
| PI6CL10804WE | W | Pb-free & Green, 8-pin 153-mil wide SOIC |

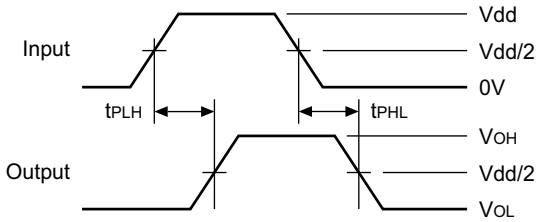
**Notes**:
1. Thermal Characteristics can be found on the web at www.pericom.com/packaging/
2. E = Pb-free and Green
3. X suffix = Tape/Reel

## Switching Waveforms

### Propagation Delay

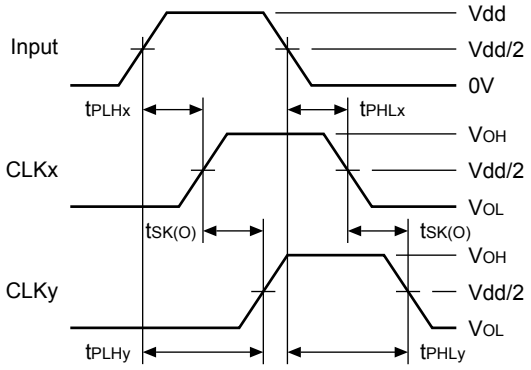



### Pulse Skew – $t_{SK(P)}$



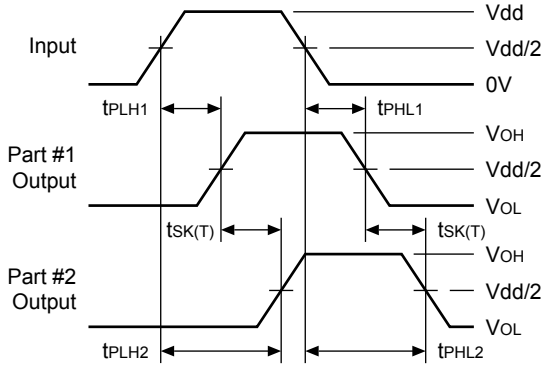

$t_{sk(p)} = | t_{PLH} - t_{PHL} |$

### Output Skew – $t_{SK(O)}$




$t_{SK(O)} = | t_{PLHy} - t_{PLHx} |$ or $| t_{PHLy} - t_{PHLx} |$

### Package Skew – $t_{SK(T)}$




$t_{SK(T)} = | t_{PLH2} - t_{PLH1} |$ or $| t_{PHL2} - t_{PHL1} |$