19-3886; Rev 1; 8/06

EVALUATION KIT AVAILABLE

VRD11/VRD10, K8 Rev F 2/3/4-Phase PWM Controllers with Integrated Dual MOSFET Drivers

General Description

The MAX8809A/MAX8810A synchronous, 2-/3-/4-phase, step-down, current-mode controllers with integrated dual-phase MOSFET drivers provide flexible solutions that fully comply with Intel® VRD11/VRD10 and AMD K8 Rev F CPU core supplies. The flexible design supplies load currents up to 150A for low-voltage CPU core power requirements.

A tri-state SEL input is available to configure the VID logic for either the Intel VRD11/VRD10 or AMD K8 Rev F applications. An enable input (EN) is available to disable the IC. True-differential remote output-voltage sensing enables precise regulation at the load by eliminating the effects of trace impedance in the output and return paths. A high-accuracy DAC combined with precision current-sense amplifiers and droop control enable the MAX8809A/MAX8810A to meet the most stringent tolerance requirements of new-generation high-current CPUs. These ICs use either integral or voltage-positioning feedback control to achieve high output-voltage accuracy.

The COMP input allows for either positive or negative voltage offsets from the VID code voltage. A power-good signal (VRREADY) is provided for startup sequencing and fault annunciation. The SS/OVP pin enables the programming of the soft-start period, and provides an indication of an overvoltage condition. A soft-stop feature prevents negative voltage spikes on the output at turn-off, eliminating the need for an external Schottky clamp diode.

The MAX8809A/MAX8810A incorporate a proprietary "rapid active average" current-mode control scheme for fast and accurate transient-response performance, as well as precise load current sharing. Either the inductor DCR or a resistive current-sensing element is used for current sensing. When used with DCR sensing, rapid active current averaging (RA^2) eliminates the tolerance effects of the inductance and associated current-sensing components, providing superior phase current matching, accurate current limit, and precise load-line.

The MAX8809A operates as a single-chip, 2-phase solution with integrated drivers. It also provides a 3rd-phase PWM output and easily supports 3-phase design by adding the MAX8552 high-performance driver. The MAX8810A enables up to 4-phase designs by adding the MAX8523 high-performance dual driver for a compact 2-chip solution.

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Features

- **VRD11/VRD10 and K8 Rev F Compliant**
- **±0.35% Initial Output Voltage Accuracy**
- **Dual Integrated Drivers with Integrated Bootstrap Diodes**
- **Up to 26V Input Voltage**
- **Adaptive Shoot-Through Protection**
- **Soft-Start, Soft-Stop, VRREADY Output**
- **Fast Load Transient Response**
- **Individual Phase, Fully Temperature-Compensated Cycle-by-Cycle Average Current Limit**
- **Current Foldback at Short Circuit**
- **Voltage Positioning or Integral Feedback**
- **Differential Remote Voltage Sensing**
- **Programmable Positive and Negative Offset Voltages**
- **150kHz to 1.2MHz Switching Frequency per Phase**
- **NTC-Based, Temperature-Independent Load Line**
- **Precise Phase Current Sharing**
- **Programmable Thermal-Monitoring Output (VRHOT)**
- **6A Peak MOSFET Drivers**
- **0.3Ω/0.85Ω Low-Side, 0.8Ω/1.1Ω High-Side Drivers (typ)**
- **40-Pin and 48-Pin Thin QFN Packages**

Applications

Desktop PCs

Servers, Workstations

Desknote and LCD PCs

Voltage-Regulator Modules

Ordering Information

PART	PIN-PACKAGE	PKG CODE	FUNCTION
MAX8809AETL+	40 Thin QFN 5mm x 5mm	T4055-1	2-/3-phase
MAX8810AETM+	48 Thin QFN 6mm x 6mm	T4866-1	2-/3-/4-phase

+Denotes lead-free package.

Note: *All parts are specified in the -40°C to +85°C extended temperature range.*

Pin Configurations appear at end of data sheet.

VRD11/VRD10, K8 Rev F 2/3/4-Phase PWM Controllers with Integrated Dual MOSFET Drivers

ABSOLUTE MAXIMUM RATINGS

REF, COMP, SS/OVP, OSC, NTC, VRTSET, RS+, RS-, PWM_ to GND ..... -0.3V to (V_{CC} + 0.3V)
CS_+, CS_-, VID_, BUF, EN, ILIM, SEL, VRREADY, VRHOT, V_{CC} to GND ..... -0.3V to +6V
BST_ to PGND_ ..... -0.3V to +35V
LX_ to PGND_ ..... -1V to +28V
BST_ to VL_ ..... -1V to +30V
DH_ to PGND_ ..... -0.3V to ($V_{BST\_}$ + 0.3V)
DH_, BST_ to LX_ ..... -0.3V to +7V
VL_ to PGND_ ..... -0.3V to +7V
DL_ to PGND_ ..... -0.3V to ($V_{VL\_}$ + 0.3V)
PGND_ to GND ..... -0.3V to +0.3V
CS_+ to CS_- ..... -0.3V to +0.3V
DH_, DL_ Current ..... ±200mA$_{RMS}$
VL_ to BST_ Diode Current ..... 50mA$_{RMS}$
Continuous Power Dissipation (T_A = +70°C)
40-Pin Thin QFN 5mm x 5mm (derate 35.7mW/°C above +70°C) 2857.1mW
48-Pin Thin QFN 6mm x 6mm (derate 37mW/°C above +70°C) 2963mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{VL\_}$ = $V_{BST\_}$ = 6.5V, V_{CC} = V_{EN} = 5V, V_{ILIM} = 1.5V, VID_ = SEL = REF = BUF = unconnected, V_{COMP} = V_{RS+} = 1.0V, $R_{VRREADY}$ = 5kΩ pullup to 5V, $R_{SS/OVP}$ = 12kΩ to GND, R_{NTC} = 10kΩ to GND, f_{SW} = 300kHz, R_{VRTSET} = 118kΩ to GND, V_{CS_+} = V_{CS_-} = 1V, PWM_ = unconnected, R_{VRHOT} = 249Ω pullup to 1.05V, V_{GND} = $V_{PGND\_}$ = $V_{LX\_}$ = V_{RS-} = 0V, DL_ = DH_ = unconnected, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Operating Range		4.5		5.5	V
V_{CC} UVLO Trip Level	Rising	4.0	4.25	4.5	V
	Falling	3.7	4.0	4.3	
V_{CC} Shutdown Supply Current	V_{CC} < 3.75V		0.35		mA
V_{CC} Standby Supply Current	V_{EN} = 0V		0.5		mA
V_{CC} Operating Supply Current	V_{RS+} - V_{RS-} = 1.0V, no switching, V_{DAC} = 1.0V (Note 1)		13		mA
Thermal Shutdown	Temperature rising, hysteresis = 25°C (typ)		+160		°C
INTERNAL REFERENCE (REF)					
Output Voltage	I_{REF} = -100µA	1.992	2.000	2.008	V
Output Regulation (Sourcing)	V_{CC} = 4.5V at I_{REF} = -500µA to V_{CC} = 5.5V at I_{REF} = -100µA	-0.05		+0.05	%
Output Regulation (Sinking)	V_{CC} = 4.5V at I_{REF} = +100µA to V_{CC} = 5.5V at I_{REF} = +500µA	-0.2		+0.2	%
Reference UVLO Trip Level	Rising (100mV typ hysteresis)		1.84		V
BUF REFERENCE					
BUF Regulation Voltage	I_{BUF} = 0A	0.99	1.0	1.01	V
BUF Output Regulation	V_{CC} = 4.5V at I_{BUF} = +100µA to V_{CC} = 5.5V at I_{BUF} = +500µA	-0.25		+0.25	%
SOFT-START					
EN Startup Delay (TD1)	From EN rising to V_{OUT} rising	1.6	2.2	2.8	ms
Soft-Start Period Range (TD2)	12kΩ < $R_{SS/OVP}$ < 90.9kΩ	0.5		6.5	ms
Soft-Start Tolerance	$R_{SS/OVP}$ = 56kΩ	2.25	3.00	3.75	ms
Intel Boot-Level Duration (TD3)	SEL = GND or SEL = V_{CC}	175	250	350	µs

ELECTRICAL CHARACTERISTICS (continued)

($V_{VL\_}$ = $V_{BST\_}$ = 6.5V, V_{CC} = V_{EN} = 5V, V_{ILIM} = 1.5V, VID_ = SEL = REF = BUF = unconnected, V_{COMP} = V_{RS+} = 1.0V, $R_{VRREADY}$ = 5kΩ pullup to 5V, $R_{SS/OVP}$ = 12kΩ to GND, R_{NTC} = 10kΩ to GND, f_{SW} = 300kHz, R_{VRTSET} = 118kΩ to GND, V_{CS_+} = V_{CS_-} = 1V, PWM_ = unconnected, R_{VRHOT} = 249Ω pullup to 1.05V, V_{GND} = $V_{PGND\_}$ = $V_{LX\_}$ = V_{RS-} = 0V, DL_ = DH_ = unconnected, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
VOLTAGE REGULATION						
RS+ Input Bias Current	V_{RS+} = 1V			0.1	1	µA
RS- Input Bias Current	V_{RS-} = 0.2V			0.1	1	µA
Output Voltage Initial Accuracy	V_{DAC} = 1V (Note 1)		-0.35		+0.35	%
Droop Accuracy	V_{DAC} = 1V (Note 1), R_{NTC} = 10kΩ	T_A = +25°C to +85°C	-3.5		+3.5	%
		T_A = -5°C to +85°C	-5.5		+5.5	
g_{MV} Amplifier Transconductance			1.94	2.00	2.06	mS
g_{MV} Gain Bandwidth Product				5		MHz
Comp Output Current	V_{DAC} - V_{RS+} = 200mV (Note 1)			385		µA
CURRENT LIMIT						
Average Current-Limit Trip Level Accuracy	V_{ILIM} = 1.5V		-6		+6	%
ILIM Input Bias Current				0.01	1	µA
ILIM Default Program Level	V_{ILIM} > V_{CC} - 0.2V		1.197	1.330	1.463	V
ENABLE INPUT (EN)						
Turn-On Threshold (Rising)	V_{CC} = 4.5V to 5.5V, 100mV typ hysteresis		0.8	0.85	0.9	V
LOGIC INPUTS (VID0–VID7)						
INTEL (SEL = HIGH OR LOW)						
Input Low Level	V_{CC} = 4.5V to 5.5V				0.4	V
Input High Level	V_{CC} = 4.5V to 5.5V		0.8			V
Input Pulldown Resistance			100		270	kΩ
AMD (SEL = UNCONNECTED)						
Input Low Level	V_{CC} = 4.5V to 5.5V				0.6	V
Input High Level	V_{CC} = 4.5V to 5.5V		1.4			V
Input Pulldown Resistance			100		270	kΩ
LOGIC INPUT (SEL)						
Internal Bias Resistance			50	100	200	kΩ
Internal Bias Voltage	V_{CC} = 4.5V to 5.5V			V_{CC} / 2		V
Input Low Level	V_{CC} = 4.5V to 5.5V				0.5	V
Input High Level	V_{CC} = 4.5V to 5.5V		V_{CC} - 0.5			V
VRREADY OUTPUT						
Output Low Level	$I_{VRREADY}$ = +4mA				0.4	V
Output High Leakage	$V_{VRREADY}$ = 5.5V				1	µA
VRREADY Blanking Time	From EN rising to VRREADY rising, $R_{SS/OVP}$ = 12kΩ		3.0		5.5	ms

VRD11/VRD10, K8 Rev F 2/3/4-Phase PWM Controllers with Integrated Dual MOSFET Drivers

ELECTRICAL CHARACTERISTICS (continued)

($V_{VL\_}$ = $V_{BST\_}$ = 6.5V, V_{CC} = V_{EN} = 5V, V_{ILIM} = 1.5V, VID_ = SEL = REF = BUF = unconnected, V_{COMP} = V_{RS+} = 1.0V, $R_{VRREADY}$ = 5kΩ pullup to 5V, $R_{SS/OVP}$ = 12kΩ to GND, R_{NTC} = 10kΩ to GND, f_{SW} = 300kHz, R_{VRTSET} = 118kΩ to GND, V_{CS_+} = V_{CS_-} = 1V, PWM_ = unconnected, R_{VRHOT} = 249Ω pullup to 1.05V, V_{GND} = $V_{PGND\_}$ = $V_{LX\_}$ = V_{RS-} = 0V, DL_ = DH_ = unconnected, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VRREADY Upper Threshold (Note 1)	(V_{RS+} - V_{RS-}) rising	V_{DAC} + 0.150		V_{DAC} + 0.200	V
	(V_{RS+} - V_{RS-}) falling	V_{DAC} + 0.075		V_{DAC} + 0.125	
VRREADY Lower Threshold (Note 1)	(V_{RS+} - V_{RS-}) falling	V_{DAC} - 0.250		V_{DAC} - 0.200	V
	(V_{RS+} - V_{RS-}) rising	V_{DAC} - 0.175		V_{DAC} - 0.125	
OVERVOLTAGE PROTECTION					
Intel (SEL = High or Low)	(V_{RS+} - V_{RS-}) rising (Note 1)	V_{DAC} + 0.150	V_{DAC} + 0.175	V_{DAC} + 0.200	V
AMD (SEL = Unconnected)	(V_{RS+} - V_{RS-}) rising	1.750	1.775	1.800	V
SS/OVP High Level	$I_{SS/OVP}$ = -10mA	V_{CC} - 0.450			V
OSCILLATOR					
Oscillator Frequency Accuracy (per Phase)	Frequency per phase = 300kHz	-10		+10	%
Switching Frequency Range (per Phase)		150		1200	kHz
CURRENT-SENSE AMPLIFIERS					
Current-Sense Amplifier Gain (G_{CA})	R_{NTC} = 10kΩ, T_A = +25°C to +85°C	28.8	30.0	31.2	V/V
CS_+ Input Bias Current	V_{CS_+} = V_{CS_-} = 2V		0.3	3.0	µA
CS_- Input Bias Current	V_{CS_+} = V_{CS_-} = 2V		0.6	5.5	µA
CS to PWM_ Delay	V_{COMP} falling		20		ns
GAIN TEMPERATURE COMPENSATION (NTC)					
Compensation Accuracy	R_{NTC} temperature = 0°C to +125°C (10k NTC Panasonic ERTJ1VR103)	-6		+6	%
VRHOT TEMPERATURE MONITORING					
VRHOT Output Low Voltage	I_{VRHOT} = +4mA			0.4	V
VRHOT Output High Leakage Current	V_{VRHOT} = 5.5V			5	µA
VRTSET Temperature Range		+60		+125	°C
VRTSET Accuracy	R_{NTC} temperature = +60°C to +125°C, 15°C hysteresis (typ) (10k NTC Panasonic ERTJ1VR103)	-5		+5	°C

ELECTRICAL CHARACTERISTICS (continued)

($V_{VL\_}$ = $V_{BST\_}$ = 6.5V, V_{CC} = V_{EN} = 5V, V_{ILIM} = 1.5V, VID_ = SEL = REF = BUF = unconnected, V_{COMP} = V_{RS+} = 1.0V, $R_{VRREADY}$ = 5kΩ pullup to 5V, $R_{SS/OVP}$ = 12kΩ to GND, R_{NTC} = 10kΩ to GND, f_{SW} = 300kHz, R_{VRTSET} = 118kΩ to GND, V_{CS_+} = V_{CS_-} = 1V, PWM_ = unconnected, R_{VRHOT} = 249Ω pullup to 1.05V, V_{GND} = $V_{PGND\_}$ = $V_{LX\_}$ = V_{RS-} = 0V, DL_ = DH_ = unconnected, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PWM DRIVER					
Output Low Level	$I_{PWM\_}$ = +5mA		0.1	0.4	V
Output High Level	$I_{PWM\_}$ = -5mA	4.5	4.9		V
Source Current	$V_{PWM\_}$ = V_{CC} - 2V		52		mA
Sink Current	$V_{PWM\_}$ = 2V		65		mA
Rise/Fall Times			10		ns
PWM Disable Program Threshold	4V < V_{CC} < 5.5V	3.0	V_{CC} - 0.7		V
GATE-DRIVER SPECIFICATIONS					
VL_, BST_ to LX_ Input Voltage Range		4.5		6.5	V
LX Operating Range				26	V
VL_ UVLO Threshold (VL12, MAX8809A; VL1, MAX8810A)	$V_{VL\_}$ rising, 250mV hysteresis (typ)	3.25	3.55	3.80	V
Driver Static Supply Current, $I_{VL\_}$ (per Channel)	DH_ = BST_		1	1.6	mA
	DH_ = LX_		1.1	1.8	
Boost Static Supply Current, $I_{BST\_}$ (per Channel)	DH_ = BST_		0.6	1	mA
DH Driver Resistance	Sourcing current, $V_{VL\_}$ = 6.5V		1.1	2.0	Ω
	Sinking current, $V_{VL\_}$ = 6.5V		0.8	1.2	
DL Driver Resistance	Sourcing current, $V_{VL\_}$ = 6.5V		0.85	1.7	Ω
	Sinking current, $V_{VL\_}$ = 6.5V		0.3	0.6	
DH_ Rise Time (t_{rDH})	$C_{DH\_}$ = 3000pF		14		ns
DH_ Fall Time (t_{fDH})	$C_{DH\_}$ = 3000pF		9		ns
DL_ Rise Time (t_{rDL})	$C_{DL\_}$ = 3000pF		10		ns
DL_ Fall Time (t_{fDL})	$C_{DL\_}$ = 3000pF		7		ns
DH_ Propagation Delay (t_{pDHf})	CS+ rising to DH falling		32		ns
Dead Time (t_{pDLr})	LX_ falling to DL_ rising		18		ns
Dead Time (t_{DEAD})	DL_ falling to DH_ rising		35		ns
INTERNAL BOOST-DIODE SPECIFICATIONS					
On-Resistance	$I_{BST\_}$ = 2mA		6		Ω

VRD11/VRD10, K8 Rev F 2/3/4-Phase PWM Controllers with Integrated Dual MOSFET Drivers

ELECTRICAL CHARACTERISTICS

($V_{VL\_}$ = $V_{BST\_}$ = 6.5V, V_{CC} = V_{EN} = 5V, V_{ILIM} = 1.5V, VID_ = SEL = REF = BUF = unconnected, V_{COMP} = V_{RS+} = 1.0V, $R_{VRREADY}$ = 5kΩ pullup to 5V, $R_{SS/OVP}$ = 12kΩ = R_{NTC} = 10kΩ to GND, f_{SW} = 300kHz, R_{VRTSET} = 50kΩ to GND, V_{CS_+} = V_{CS_-} = 1V, PWM_ = unconnected, R_{VRHOT} = 249Ω pullup to 1.05V, V_{GND} = $V_{PGND\_}$ = $V_{LX\_}$ = V_{RS-} = 0V, DL_ = DH_ = unconnected, **T_A = -40°C to +85°C**.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Operating Range		4.5		5.5	V
V_{CC} UVLO Trip Level	Rising	4.0		4.5	V
	Falling	3.7		4.3	
INTERNAL REFERENCE (REF)					
Output Voltage	I_{REF} = -100µA	1.99		2.01	V
Output Regulation (Sourcing)	V_{CC} = 4.5V at I_{REF} = -500µA to V_{CC} = 5.5V at I_{REF} = -100µA	-0.065		+0.065	%
Output Regulation (Sinking)	V_{CC} = 4.5V at I_{REF} = +100µA to V_{CC} = 5.5V at I_{REF} = +500µA	-0.2		+0.2	%
BUF REFERENCE					
BUF Regulation Voltage	I_{BUF} = 0A	0.99		1.01	V
BUF Output Regulation	V_{CC} = 4.5V at I_{BUF} = +100µA to V_{CC} = 5.5V at I_{REF} = +500µA	-0.4		+0.4	%
SOFT-START					
EN Startup Delay (TD1)	From EN rising to V_{OUT} rising	1.6		2.8	ms
Soft-Start Period Range (TD2)	12kΩ < $R_{SS/OVP}$ < 90.9kΩ	0.5		6.5	ms
Soft-Start Tolerance	$R_{SS/OVP}$ = 56kΩ	2.25		3.75	ms
Intel Boot Level Duration (TD3)	SEL = GND or SEL = V_{CC}	175		350	µs
VOLTAGE REGULATION					
RS+ Input Bias Current	V_{RS+} = 1.0V			1	µA
RS- Input Bias Current	V_{RS-} = 0.2V			1	µA
Output-Voltage Initial Accuracy	$V_{DAC\_}$ = 1V (Note 1)	-0.35		+0.35	%
g_{MV} Amplifier Transconductance		1.91		2.06	mS
CURRENT LIMIT					
Average Current-Limit Trip-Level Accuracy	V_{ILIM} = 1.5V	-11		+11	%
ILIM Input Bias Current				1	µA
ILIM Default Program Level	V_{ILIM} > V_{CC} - 0.2V	1.197		1.463	V
ENABLE INPUT (EN)					
Turn-On Threshold (Rising)	V_{CC} = 4.5V to 5.5V, 100mV typ hysteresis	0.8		0.9	V
LOGIC INPUTS (VID0–VID7)					
INTEL (SEL = HIGH OR LOW)					
Input Low Level	V_{CC} = 4.5V to 5.5V			0.4	V
Input High Level	V_{CC} = 4.5V to 5.5V	0.8			V
Input Pulldown Resistance		100		270	kΩ

ELECTRICAL CHARACTERISTICS (continued)

($V_{VL\_}$ = $V_{BST\_}$ = 6.5V, V_{CC} = V_{EN} = 5V, V_{ILIM} = 1.5V, VID_ = SEL = REF = BUF = unconnected, V_{COMP} = V_{RS+} = 1.0V, $R_{VRREADY}$ = 5kΩ pullup to 5V, $R_{SS/OVP}$ = 12kΩ = R_{NTC} = 10kΩ to GND, f_{SW} = 300kHz, R_{VRTSET} = 50kΩ to GND, V_{CS_+} = V_{CS_-} = 1V, PWM_ = unconnected, R_{VRHOT} = 249Ω pullup to 1.05V, V_{GND} = $V_{PGND\_}$ = $V_{LX\_}$ = V_{RS-} = 0V, DL_ = DH_ = unconnected, **T_A = -40°C to +85°C**.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AMD (SEL = UNCONNECTED)					
Input Low Level	V_{CC} = 4.5V to 5.5V			0.6	V
Input High Level	V_{CC} = 4.5V to 5.5V	1.4			V
Input Pulldown Resistance		100		270	kΩ
LOGIC INPUT (SEL)					
Internal Bias Resistance		50		200	kΩ
Input Low Level	V_{CC} = 4.5V to 5.5V			0.5	V
Input High Level	V_{CC} = 4.5V to 5.5V	V_{CC} - 0.5			V
VRREADY OUTPUT					
Output Low Level	$I_{VRREADY}$ = +4mA			0.4	V
Output High Leakage	$V_{VRREADY}$ = 5.5V			1	µA
VRREADY Blanking Time	From EN rising to VRREADY rising, $R_{SS/OVP}$ = 12kΩ	3.0		5.5	ms
VRREADY Upper Threshold (Note 1)	(V_{RS+} - V_{RS-}) rising	V_{DAC} + 0.150		V_{DAC} + 0.200	V
	(V_{RS+} - V_{RS-}) falling	V_{DAC} + 0.075		V_{DAC} + 0.125	
VRREADY Lower Threshold (Note 1)	(V_{RS+} - V_{RS-}) falling	V_{DAC} - 0.250		V_{DAC} - 0.200	V
	(V_{RS+} - V_{RS-}) rising	V_{DAC} - 0.175		V_{DAC} - 0.125	
OVERVOLTAGE PROTECTION					
Intel (SEL = High or Low)	(V_{RS+} - V_{RS-}) rising (Note 1)	V_{DAC} + 0.150		V_{DAC} + 0.200	V
AMD (SEL = Unconnected)	(V_{RS+} - V_{RS-}) rising	1.75		1.80	V
SS/OVP High Level	$I_{SS/OVP}$ = 10mA	V_{CC} - 0.450			V
OSCILLATOR					
Oscillator Frequency Accuracy (per Phase)	Frequency per phase = 300kHz	-20		+20	%
Switching Frequency Range (per Phase)		150		1200	kHz

VRD11/VRD10, K8 Rev F 2/3/4-Phase PWM Controllers with Integrated Dual MOSFET Drivers

ELECTRICAL CHARACTERISTICS (continued)

($V_{VL\_}$ = $V_{BST\_}$ = 6.5V, V_{CC} = V_{EN} = 5V, V_{ILIM} = 1.5V, VID_ = SEL = REF = BUF = unconnected, V_{COMP} = V_{RS+} = 1.0V, $R_{VRREADY}$ = 5kΩ pullup to 5V, $R_{SS/OVP}$ = 12kΩ = R_{NTC} = 10kΩ to GND, f_{SW} = 300kHz, R_{VRTSET} = 50kΩ to GND, V_{CS_+} = V_{CS_-} = 1V, PWM_ = unconnected, R_{VRHOT} = 249Ω pullup to 1.05V, V_{GND} = $V_{PGND\_}$ = $V_{LX\_}$ = V_{RS-} = 0V, DL_ = DH_ = unconnected, **T_A = -40°C to +85°C**.) (Note 2)

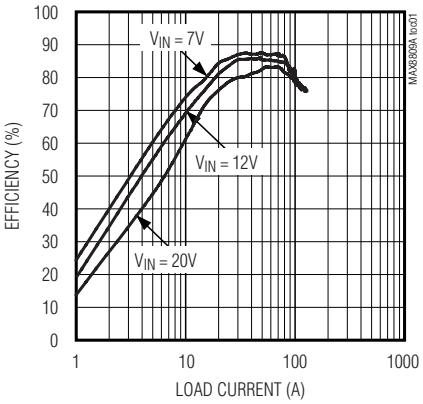
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT-SENSE AMPLIFIERS					
Current-Sense Amplifier Gain (G_{CA})	R_{NTC} = 10kΩ	27		33	V/V
CS_+ Input Bias Current	V_{CS_+} = V_{CS_-} = 2V			4.5	µA
CS_- Input Bias Current	V_{CS_+} = V_{CS_-} = 2V			7	µA
GAIN TEMPERATURE COMPENSATION (NTC)					
Temperature Compensation Accuracy	R_{NTC} temperature = 0°C to +125°C (10k NTC Panasonic ERTJ1VR103)	-7.5		+7.5	%
VRHOT TEMPERATURE MONITORING					
VRHOT Output Low Voltage	4mA sink current			0.4	V
VRHOT Output High Leakage Current	V_{VRHOT} = 5.5V			5	µA
VRTSET Temperature Range		+60		+125	°C
VRTSET Accuracy	R_{NTC} temperature = +60°C to +125°C (10k NTC Panasonic ERTJ1VR103)	-5		+5	°C
PWM DRIVER					
Output Low Level	$I_{PWM\_}$ = +5mA			0.4	V
Output High Level	$I_{PWM\_}$ = -5mA	4.5			V
PWM Disable Program Threshold	4V < V_{CC} < 5.5V	3			V
GATE-DRIVER SPECIFICATIONS					
VL_, BST_ to LX_ Input Voltage Range		4.5		6.5	V
LX_ Operating Range				26	V
VL_ UVLO Threshold (MAX8809A, VL12; MAX8810A, VL1)	$V_{VL\_}$ rising, 250mV hysteresis (typ)	3.25		3.80	V
Driver Static Supply Current, $I_{VL\_}$ (per Channel)	DH_ = BST_			1.6	mA
	DH_ = LX_			1.8	
Boost Static Supply Current, $I_{BST\_}$ (per Channel)	DH_ = BST_			1	mA
DH_ Driver Resistance	Sourcing current, $V_{VL\_}$ = 6.5V			2.0	Ω
	Sinking current, $V_{VL\_}$ = 6.5V			1.2	
DL_ Driver Resistance	Sourcing current, $V_{VL\_}$ = 6.5V			1.7	Ω
	Sinking current, $V_{VL\_}$ = 6.5V			0.6	

Note 1: V_{DAC} refers to the internal voltage set by the VID code.
Note 2: Specifications to -40°C are guaranteed by design and characterization.

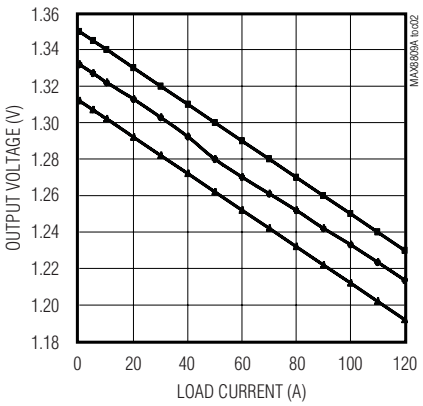
Typical Operating Characteristics

(Circuit of Figure 14, V_{IN} = 12V, V_{OUT} = 1.35V, I_{OUT_MAX} = 115A, R_O = 1mΩ, f_{SW} = 200kHz, V_{CC} = 5V, $V_{VL\_}$ = 6.5V, T_A = +25°C, unless otherwise noted.)

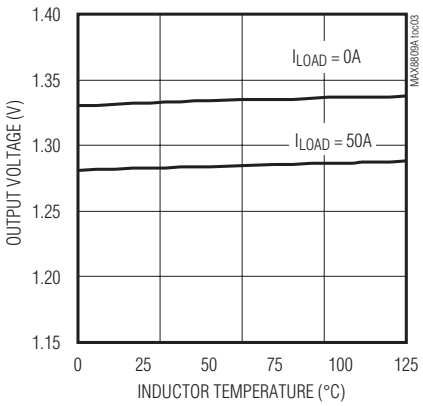
EFFICIENCY vs. LOAD CURRENT
R_{OSC} = 130kΩ



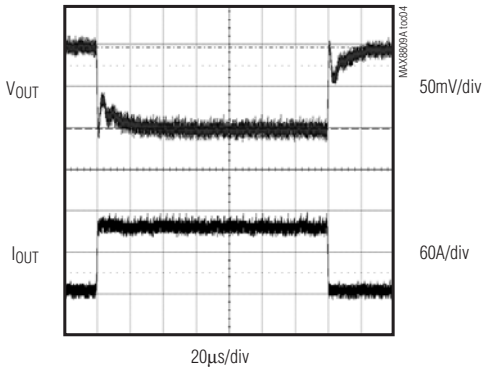
OUTPUT VOLTAGE vs. LOAD CURRENT



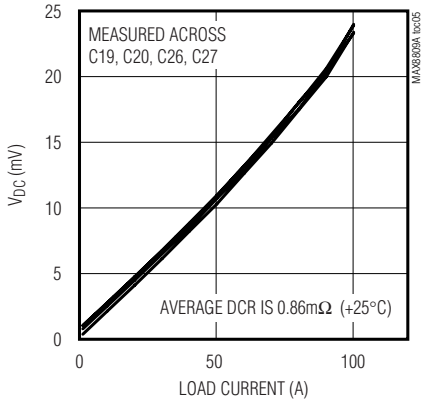
OUTPUT VOLTAGE vs. INDUCTOR TEMPERATURE



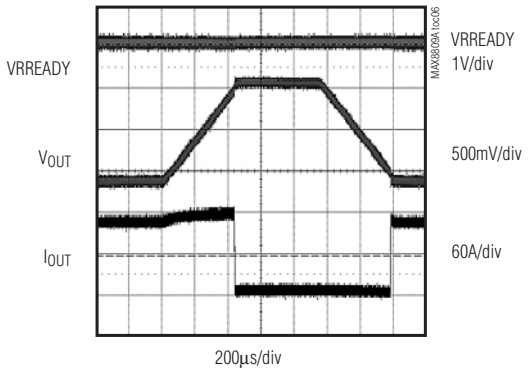
OUTPUT LOAD TRANSIENT



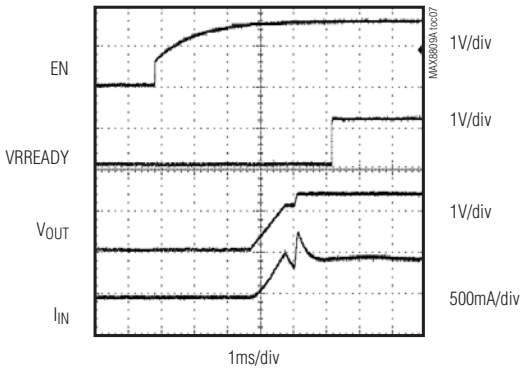
ACTIVE CURRENT SHARING vs. LOAD CURRENT



DYNAMIC VID RESPONSE



SOFT-START WAVEFORMS (INTEL)

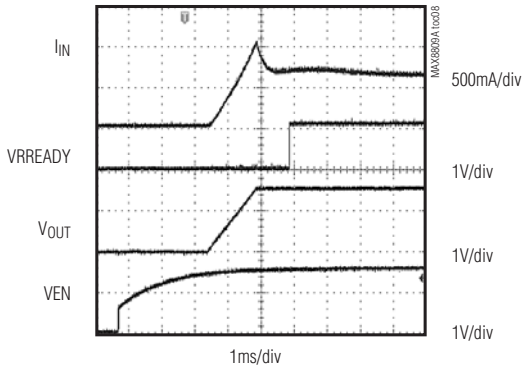


VRD11/VRD10, K8 Rev F 2/3/4-Phase PWM Controllers with Integrated Dual MOSFET Drivers

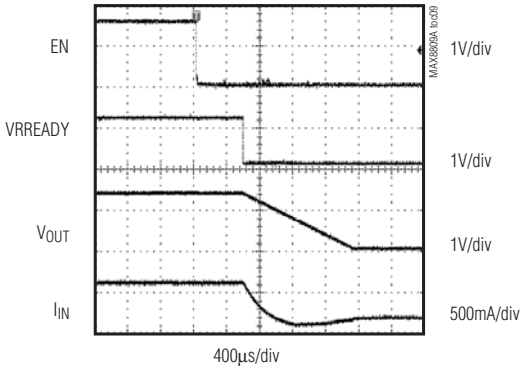
Typical Operating Characteristics (continued)

(Circuit of Figure 14, V_{IN} = 12V, V_{OUT} = 1.35V, I_{OUT_MAX} = 115A, R_O = 1mΩ, f_{SW} = 200kHz, V_{CC} = 5V, $V_{VL\_}$ = 6.5V, T_A = +25°C, unless otherwise noted.)

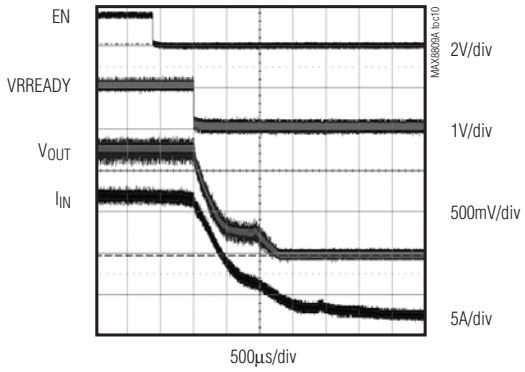
SOFT-START WAVEFORMS (AMD)



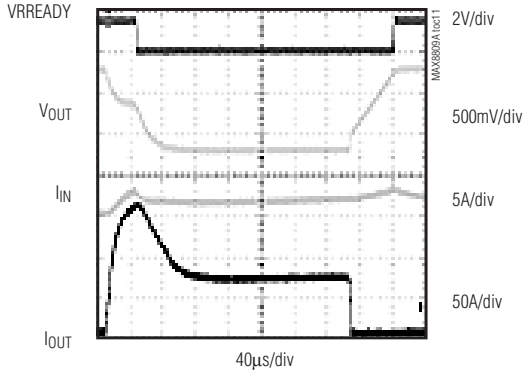
SHUTDOWN WAVEFORMS AT NO LOAD



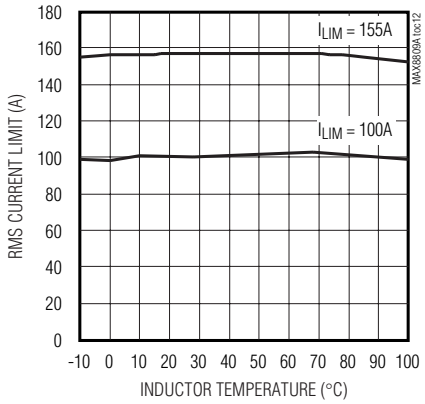
SHUTDOWN WAVEFORMS AT FULL LOAD



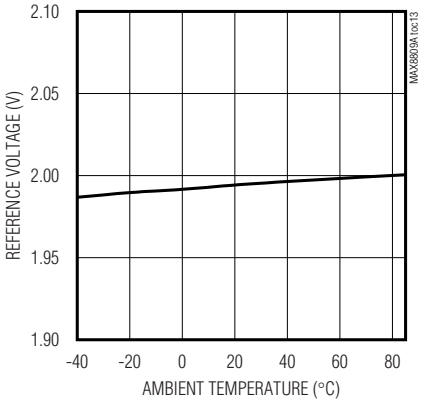
SHORT-CIRCUIT AND RECOVERY WAVEFORMS



CURRENT THRESHOLD vs. INDUCTOR CASE TEMPERATURE



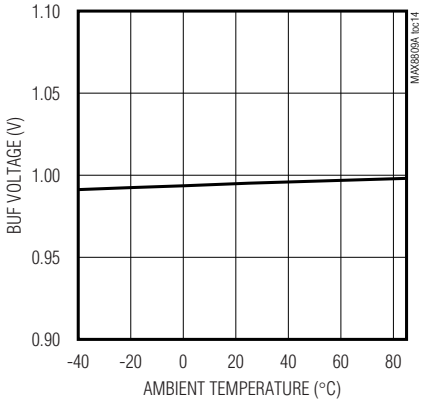
REFERENCE VOLTAGE vs. AMBIENT TEMPERATURE



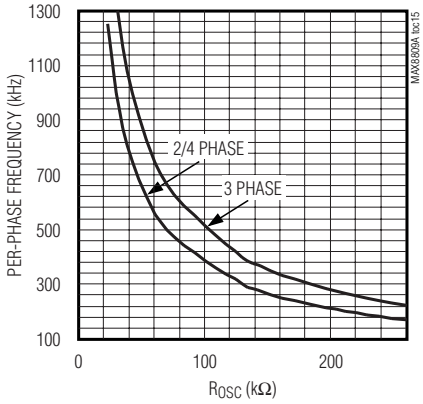
Typical Operating Characteristics (continued)

(Circuit of Figure 14, V_{IN} = 12V, V_{OUT} = 1.35V, I_{OUT_MAX} = 115A, R_O = 1mΩ, f_{SW} = 200kHz, V_{CC} = 5V, $V_{VL\_}$ = 6.5V, T_A = +25°C, unless otherwise noted.)

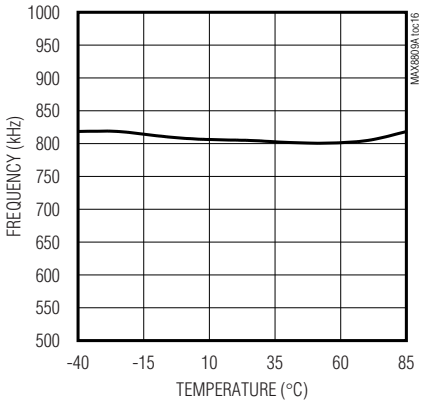
BUF VOLTAGE vs. AMBIENT TEMPERATURE



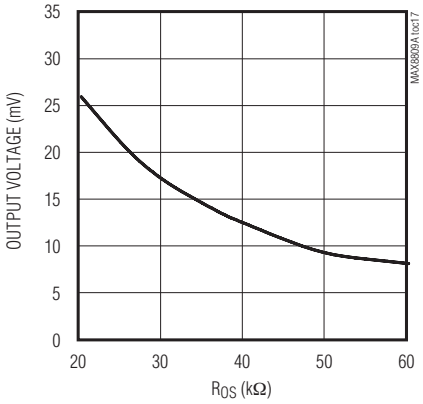
PER-PHASE FREQUENCY vs. R_{OSC}



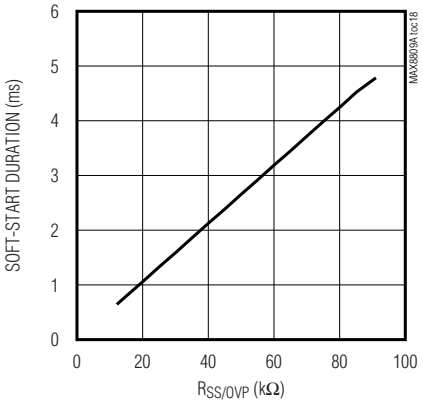
CLOCK FREQUENCY vs. TEMPERATURE



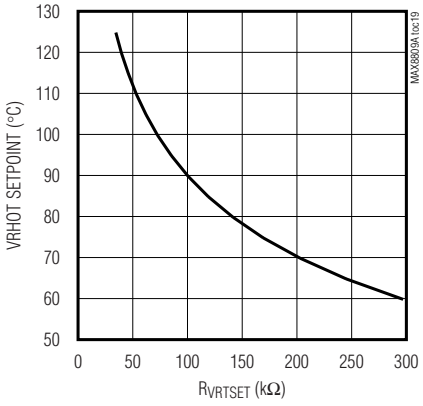
OUTPUT VOLTAGE OFFSET vs. R_{OS}



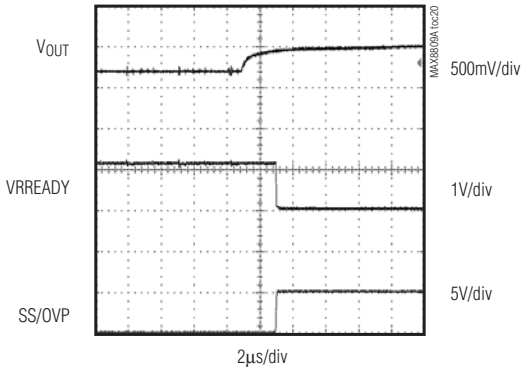
SOFT-START DURATION vs. $R_{SS/OVP}$



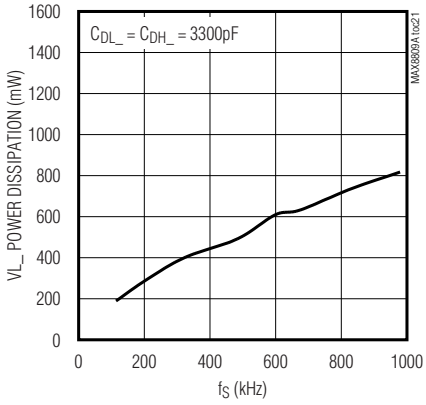
VRHOT SETPOINT vs. R_{VRTSET}



OUTPUT OVERVOLTAGE PROTECTION WAVEFORM



VL_ POWER DISSIPATION vs. PER-PHASE SWITCHING FREQUENCY

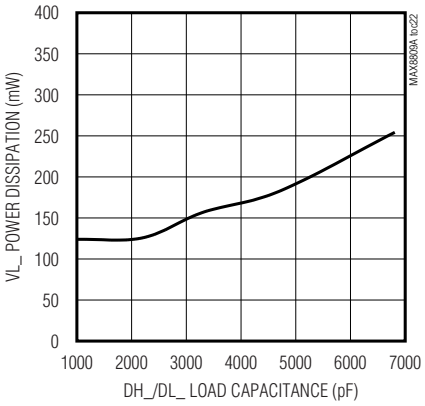


VRD11/VRD10, K8 Rev F 2/3/4-Phase PWM Controllers with Integrated Dual MOSFET Drivers

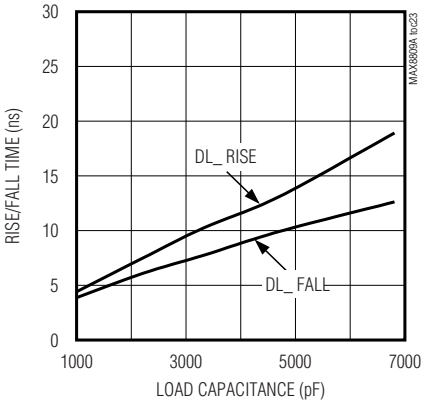
Typical Operating Characteristics (continued)

(Circuit of Figure 14, V_{IN} = 12V, V_{OUT} = 1.35V, I_{OUT_MAX} = 115A, R_O = 1mΩ, f_{SW} = 200kHz, V_{CC} = 5V, $V_{VL\_}$ = 6.5V, T_A = +25°C, unless otherwise noted.)

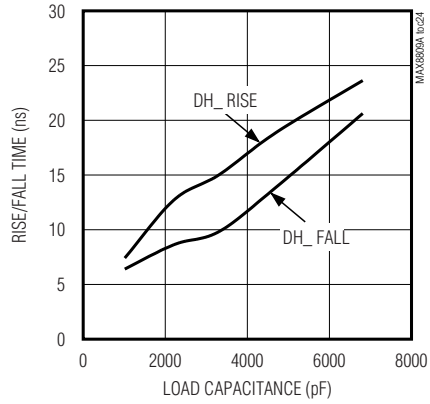
VL_ POWER DISSIPATION vs. LOAD CAPACITANCE



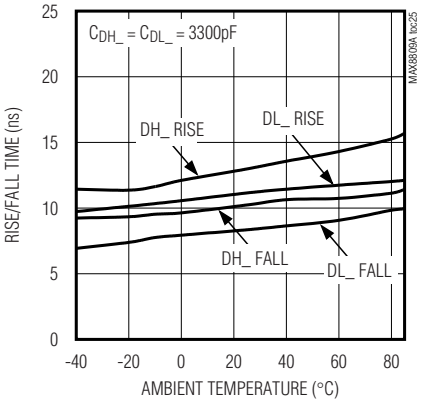
DL_ RISE/FALL TIME vs. LOAD CAPACITANCE



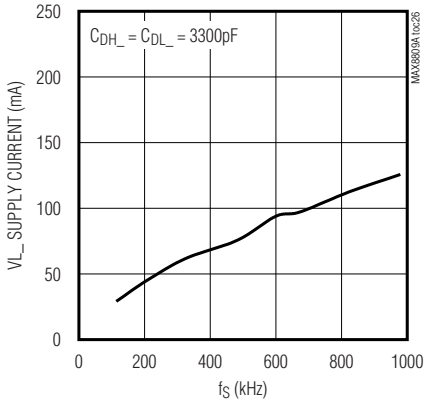
DH_ RISE/FALL TIME vs. LOAD CAPACITANCE



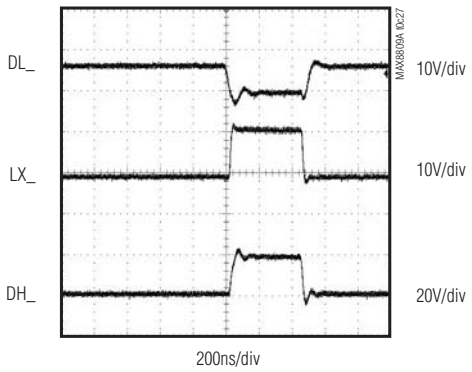
DH_/DL_ RISE/FALL TIME vs. AMBIENT TEMPERATURE



VL_ SUPPLY CURRENT vs. PER-PHASE SWITCHING FREQENCY



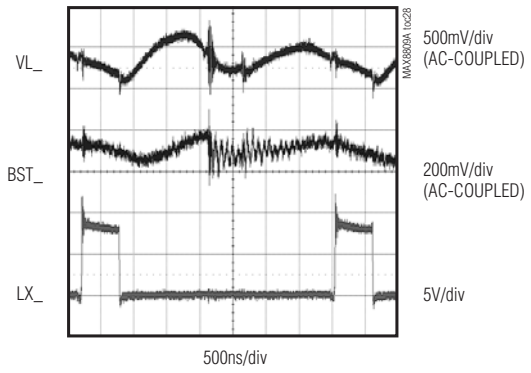
SWITCHING WAVEFORMS



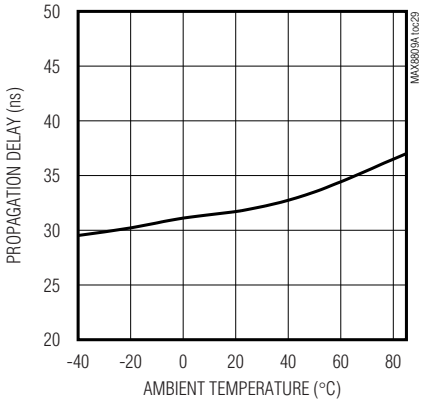
Typical Operating Characteristics (continued)

(Circuit of Figure 14, V_{IN} = 12V, V_{OUT} = 1.35V, I_{OUT_MAX} = 115A, R_O = 1mΩ, f_{SW} = 200kHz, V_{CC} = 5V, $V_{VL\_}$ = 6.5V, T_A = +25°C, unless otherwise noted.)

BST_ AND VL_ WAVEFORMS
V_{IN} = 8V



DH_ FALLING PROPAGATION DELAY vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
MAX8809A	MAX8810A		
1	48	VRREADY	Open-Drain, Power-Okay Indicator. VRREADY is an open-drain output that goes high impedance when the output is in regulation. VRREADY pulls low when the output is out of regulation, the IC is in shutdown, or V_{CC} is below the UVLO threshold.
2	1	ILIM	Current-Limit Set Input. Connect to the center tap of an external resistor-divider from REF to GND to set the cycle-by-cycle average current-limit threshold. Connect ILIM to V_{CC} to select the default current-limit threshold.
3	2	REF	Internal Reference Output. REF regulates to 2V. Bypass REF to GND with a 0.1µF to 1µF ceramic capacitor. Do not use a capacitor greater than 1µF. REF sources up to 500µA for external loads. REF is enabled when V_{CC} is above UVLO regardless of the state of EN.
4	3	COMP	Error-Amplifier Output. Connect COMP to the compensation network to implement either voltage positioning or integral feedback-control. Connect a resistor from COMP to GND to set the offset voltage. See the *Loop-Compensation Design* section for details on determining the compensation network.
5	5	GND	Analog Ground. Connect GND to the analog ground plane.
6	6	V_{CC}	IC Supply Input. Connect V_{CC} to a 4.5V to 5.5V power supply. Bypass V_{CC} to GND with a 1µF or larger ceramic capacitor.
7	8	RS-	Output-Voltage Remote-Sense Negative Input. Connect RS- to the V_{SS_SEN} remote-sense point at the load when using the remote sense. Otherwise, connect RS- to GND at the load.
8	9	RS+	Output-Voltage Remote-Sense Positive Input. Connect RS+ to the V_{CC_SEN} remote-sense point at the load when using remote sense. Otherwise, connect RS+ to the output at the load.

VRD11/VRD10, K8 Rev F 2/3/4-Phase PWM Controllers with Integrated Dual MOSFET Drivers

Pin Description (continued)

PIN		NAME	FUNCTION
MAX8809A	MAX8810A		
9	11	OSC	Internal Clock Oscillator Frequency Set Input. Connect a resistor from OSC to GND to set the internal oscillator frequency. See the *Setting the Switching Frequency* section for determining the resistor value.
10	12	SS/OVP	Soft-Start Program Input and Overvoltage-Protection Fault Flag. Connect a resistor from SS/OVP to GND to set the soft-start period. SS/OVP pulls to V_{CC} during an OVP event to signal the fault condition. See the *Soft-Start* section for determining the resistor value.
11	13	VRTSET	Temperature Comparator Program Input. Connect a resistor from VRTSET to GND to set the VRHOT temperature threshold. Connect VRTSET to V_{CC} to disable the VRHOT monitoring feature. See the *Temperature Monitoring (VRTSET, VRHOT)* section for resistor selection.
12	14	NTC	Temperature-Sensing Input. Connect a 10kΩ NTC thermistor between NTC and GND for load-line independent temperature compensation. Connect NTC to V_{CC} to disable the temperature compensation and VRHOT monitoring features. See the *Temperature Monitoring (VRTSET, VRHOT)* section for more details on selection of the NTC device.
13	—	CS3-	Phase 3 Current-Sense Negative Input. Connect to the load side of the output current-sensing element.
14	17	CS3+	Phase 3 Current-Sense Positive Input. Connect CS3+ to the positive side of the output current-sense resistor, or the positive side of the filtering capacitor if inductor DCR current sensing is used.
15	18	CS2+	Phase 2 Current-Sense Positive Input. Connect CS2+ to the positive side of the output current-sense resistor, or the positive side of the filtering capacitor if inductor DCR current sensing is used.
16	19	CS12-	Phases 1 and 2 Current-Sense Common Negative Input. Connect to the load side of the output current-sensing elements.
17	20	CS1+	Phase 1 Current-Sense Positive Input. Connect CS1+ to the positive side of the output current-sense resistor, or the positive side of the filtering capacitor if inductor DCR current sensing is used.
18	21	EN	Enable Input. Drive EN high to enable the IC. Drive EN low to place the IC in shutdown mode. If V_{CC} is greater than the UVLO threshold, EN is internally pulled to V_{CC} with a 100kΩ resistor. If V_{CC} is less than the UVLO threshold, EN is internally pulled to GND with a 2kΩ resistor.
19	23	PWM3	PWM Signal Output for phase 3. PWM3 is low during shutdown, UVLO, and OVP faults. Connect PWM3 to V_{CC} to enable 2-phase operation.
20	24	VRHOT	Temperature Fault Flag. VRHOT is an active-high, open-drain output that goes high impedance when the temperature sensed by the thermistor at NTC exceeds the temperature threshold programmed at VRTSET.
21	25	DH1	Phase 1 High-Side MOSFET Gate-Drive Output. Connect to the gate of the high-side MOSFET for phase 1. DH1 is pulled low during shutdown, UVLO, and OVP faults.
22	26	LX1	Phase 1 Inductor Sense Point. Connect LX1 to the switched side of the inductor for phase 1.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX8809A	MAX8810A		
23	27	BST1	Phase 1 High-Side MOSFET Gate-Drive Supply. Connect a 0.22µF or larger ceramic capacitor from BST1 to LX1 to supply gate drive for the high-side MOSFET. See the *Boost Capacitor Selection* section for details on calculating the BST1 capacitor value.
24	28	DL1	Phase 1 Low-Side MOSFET Gate-Drive Output. Connect to the gate of the low-side MOSFET for phase 1. DL1 is pulled low during undervoltage lockout and pulled high during an OVP fault. DL1 is high in shutdown if V_{CC} is greater than the UVLO threshold.
25	29	PGND1	Power Ground for the Phase 1 Driver. Connect PGND1 to the source of the phase 1 low-side MOSFET. PGND1 must be connected to PGND2 and GND externally. See the *PC Board Layout Guidelines* section for more details.
26	—	VL12	Phase 1 and 2 Low-Side MOSFET Gate-Drive Supply. Connect VL12 to a 4.5V to 6.5V supply. Bypass VL12 with a 2.2µF or larger ceramic capacitor to the power ground plane.
27	32	PGND2	Power Ground for the Phase 2 Driver. Connect PGND2 to the source of the phase 2 low-side MOSFET. PGND2 must be connected to PGND1 and GND externally. See the *PC Board Layout Guidelines* section for more details.
28	33	DL2	Phase 2 Low-Side MOSFET Gate-Drive Output. Connect to the gate of the low-side MOSFET for phase 2. DL2 is pulled low during undervoltage lockout and pulled high during an OVP fault. DL2 is high in shutdown if V_{CC} is greater than the UVLO threshold.
29	34	BST2	Phase 2 High-Side MOSFET Gate-Drive Supply. Connect a 0.22µF or larger ceramic capacitor from BST2 to LX2 to supply gate drive for the high-side MOSFET. See the *Boost Capacitor Selection* section for details on calculating the BST2 capacitor value.
30	35	LX2	Phase 2 Inductor Sense Point. Connect LX2 to the switched side of the inductor for phase 2.
31	36	DH2	Phase 2 High-Side MOSFET Gate-Drive Output. Connect to the gate of the high-side MOSFET for Phase 2. DH2 is pulled low during shutdown, UVLO, and OVP faults.
32	38	SEL	VID Table Selection Input. Connect SEL to GND to select the VRD10 VID code (Table 5). Connect SEL to V_{CC} to select the VRD11 8-bit VID code (Table 6). Leave SEL unconnected to select the K8 Rev F VID code (Table 4).
33–40	39–46	VID7–VID0	Voltage Identification Code Inputs. Use VID_ to set the output voltage. SEL selects the VRD10, VRD11, or K8 Rev F VID logic codes. Connect VID_ to the system V_{TT} with a 680Ω resistor for logic-high for Intel VR solutions. Connect VID_ to the system V_{DDQ} with a 1kΩ resistor for logic-high for AMD VR solutions.

VRD11/VRD10, K8 Rev F 2/3/4-Phase PWM Controllers with Integrated Dual MOSFET Drivers

Pin Description (continued)

PIN		NAME	FUNCTION
MAX8809A	MAX8810A		
—	4	BUF	1V Reference Output. Bypass BUF to GND with a 1µF or larger ceramic capacitor. Connect a resistor from COMP to BUF to set the load-line. See the *Loop-Compensation Design* section for more details.
—	7, 10, 37, 47	N.C.	No Internal Connection
—	15	CS4+	Phase 4 Current-Sense Positive Input. Connect CS4+ to the positive side of the output current-sense resistor, or the positive side of the filtering capacitor if inductor DCR current sensing is used.
—	16	CS34-	Phases 3 and 4 Current-Sense Common Negative Input. Connect to the load side of the output current-sensing elements.
—	22	PWM4	PWM Signal Output for Phase 4. PWM4 is low during shutdown, UVLO, and OVP faults. Connect PWM4 to V_{CC} to enable 3-phase operation. Connect PWM3 and PWM4 to V_{CC} to enable 2-phase operation.
—	30	VL1	Phase 1 Low-Side MOSFET Gate-Drive Supply. Connect VL1 to a 4.5V to 6.5V supply. VL1 must be connected to VL2 externally. Bypass the VL1/VL2 connection with a 2.2µF or larger ceramic capacitor to the power ground plane.
—	31	VL2	Phase 2 Low-Side MOSFET Gate-Drive Supply. Connect VL2 to a 4.5V to 6.5V supply. VL2 must be connected to VL1 externally. Bypass the VL1/VL2 connection with a 2.2µF or larger ceramic capacitor to the power ground plane.
—	—	EP	Exposed Paddle. Connect to the analog GND plane for enhanced thermal power dissipation.

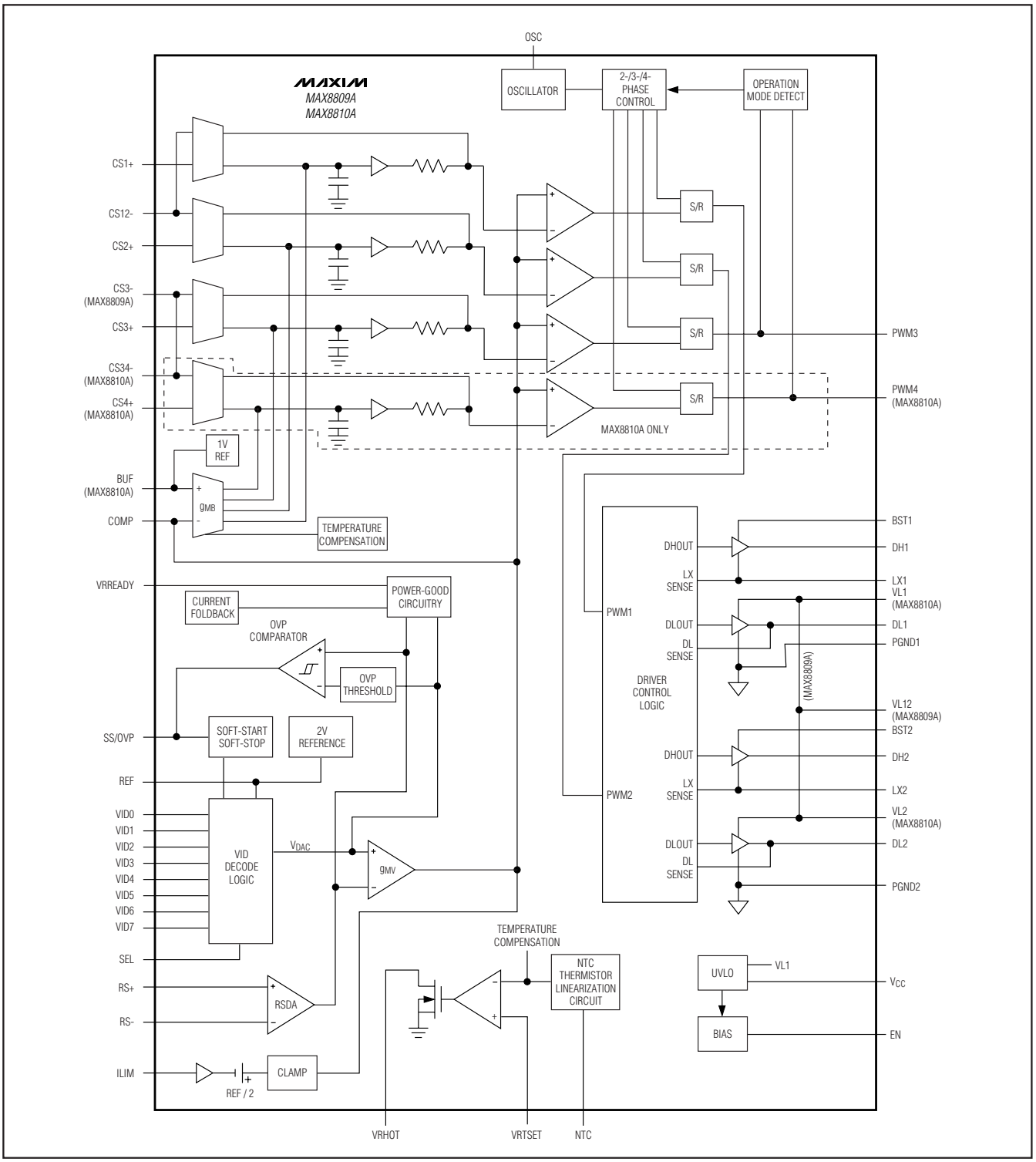


Figure 1. Block Diagram

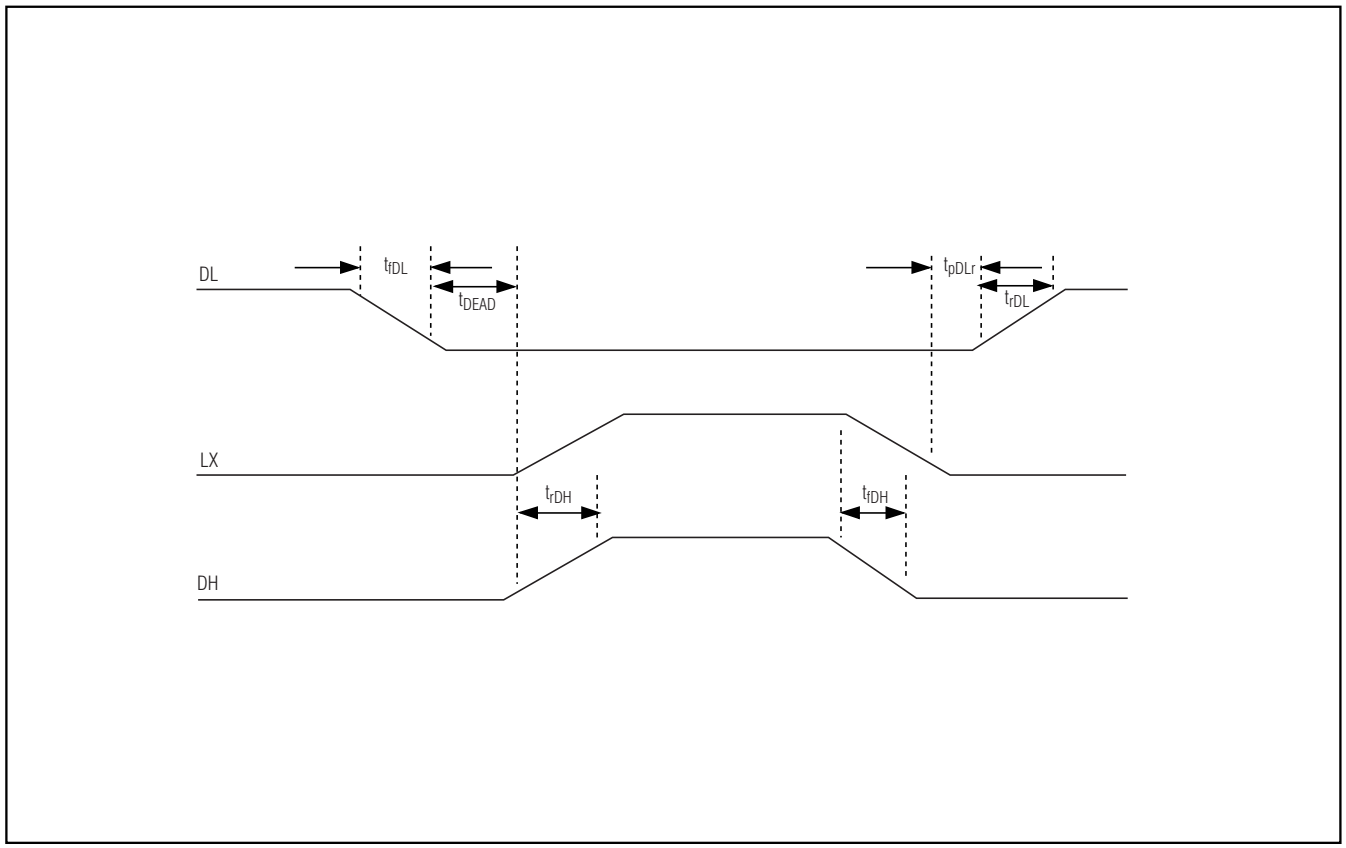


Figure 2. Driver Timing Diagram

Detailed Description

The MAX8809A/MAX8810A synchronous, 2-/3-/4-phase, step-down, current-mode controllers with integrated dual-phase MOSFET drivers provide flexible solutions that fully comply with Intel VRD11/VRD10 and AMD K8 Rev F CPU core supplies. The flexible design supplies load currents of up to 150A for low-voltage CPU core power supplies.

The MAX8809A is suitable for 2- or 3-phase core supply applications. With an integrated dual-MOSFET driver, the MAX8809A offers a single-chip IC solution for dual-phase core supplies. Together with the MAX8552, a high-performance single-phase MOSFET driver, the MAX8809A also supports 3-phase core supplies. Similarly, the MAX8810A features a single IC solution for dual-phase core supplies. It also features two-IC solutions for 3- or 4-phase core supplies by adding a single MOSFET driver (MAX8552) or a dual-MOSFET driver (MAX8523).

Both the MAX8809A and MAX8810A fully comply with Intel VRD11, Extended VRD10, and the AMD K8 Rev F VID codes. The SEL input allows the user to select the architecture specifications.

Clock Frequency (OSC)

An external resistor, R_{OSC}, from OSC to GND sets the internal clock frequency of the MAX8809A/MAX8810A. A 1% resistor is recommended to maintain good frequency accuracy. The internal clock frequency sets the per-phase switching frequency. The selection of switching frequency per phase is influenced by factors such as the switching speed of the MOSFETs, the inductor's core material, different types of input and output capacitors, and the available board space. Once the per-phase switching frequency is selected, the internal clock frequency is determined using the procedure in the *Setting the Switching Frequency* section.

Voltage Reference (REF)

A precision 2V reference is provided by the MAX8809A/MAX8810A at the REF output. REF is capable of sinking and sourcing up to 500µA for external loads. Connect a 0.1µF to 1µF ceramic capacitor from REF to GND. Internal REFOK circuitry monitors the reference voltage. The reference voltage must be above the REFOK threshold of 1.84V to activate the controller. The controller is disabled if the reference voltage falls below 1.74V.

Output Current Sensing (CS_+, CS_-)

The output current of each phase is sensed differentially. A low-offset-voltage, differential-current amplifier (30V/V) at each phase allows low-resistance current-sense resistors to be used to minimize power dissipation. Sensing the current at the output of each phase offers advantages including less noise sensitivity, more accurate current sharing between phases, and the flexibility of using either a current-sense resistor or the DC resistance of the output inductor.

Using the DC resistance, R_{DC}, of the output inductor (Figure 3) allows higher efficiency. In this configuration, the initial tolerance and temperature coefficient of R_{DC} must be accounted for in the output-voltage droop-error budget. The temperature coefficient can be compensated; see the *Load-Line Independent Inductor DC Resistance Temperature Compensation* section for more details. An RC-filtering network is needed to extract the current information from the output inductor. The time constant of the RC network is calculated as follows:

$$R1 \times C1 = \frac{L}{R_{DC}}$$

where L is the inductance of the output inductor. For 20A or higher current-per-phase applications, the DC resistance of commercially available inductors is approximately 1mΩ. To minimize current-sense error due to the bias current at the current-sense inputs, choose R1 less than 2kΩ. Determine the value for C1 as:

$$C1 = \frac{L}{(R_{DC} \times R1)}$$

Select a 1% resistor for R1. For mainstream PCs 20% tolerance is recommended for C1, and for performance PCs 10% tolerance should be considered. If using an inductor with R_{DC} greater than 1mΩ, a resistor (R2) may be necessary to divide down the voltage across CS_+ and CS_-. The maximum average signal present at the input of the current-sense amplifier should not exceed 85mV.

When a current-sense resistor is used for more accurate current sharing and load-line, a similar RC-filtering circuit is recommended to cancel the equivalent series inductance of the current-sense resistor, as shown in Figure 4. Again, select R2 less than 2kΩ, and C2 is determined by the following equation:

$$C2 = \frac{ESL}{(R_S \times R2)}$$

where ESL is the equivalent series inductance of the current-sense resistor and R_S is the value of the current-sense resistor. For example, a 1mΩ, 2025 package sense resistor has an ESL of 1.6nH. If using an R_S greater than 1mΩ, a resistor (R2) may be necessary to divide down the voltage across CS_+ and CS_-. The maximum average signal present at the input of the current-sense amplifier should not exceed 85mV.

Output Current Limit and Short-Circuit Protection (ILIM)

The MAX8809A/MAX8810A feature a precise average output current limit on a cycle-by-cycle basis using Maxim's proprietary RA² technology. The current-limit scheme is insensitive to input-voltage variation, the inductor tolerance, and the tolerance of the current-sense capacitor, permitting the use of low-cost components to reduce total BOM cost. Furthermore, the current limit is fully temperature compensated resulting

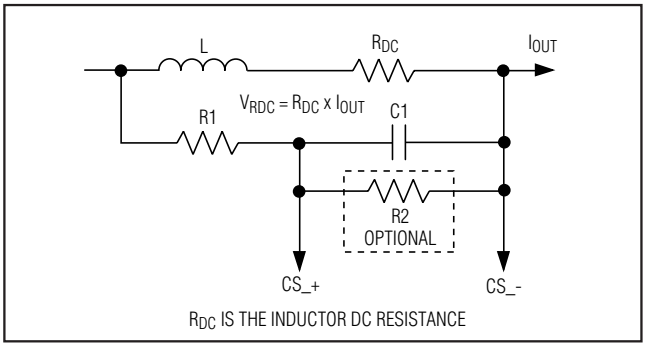


Figure 3. Inductor R_{DC} Current Sense

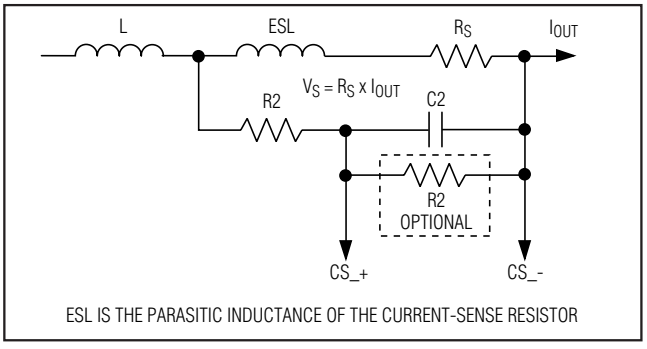


Figure 4. Resistor Current Sense

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in a constant output current limit over the entire operational temperature range. This eliminates the need to oversize MOSFETs and inductors to compensate for thermal effects. Connecting ILIM to V_{CC} programs the default current-limit threshold. To select a different current-limit threshold, connect a resistor-divider from REF to GND with ILIM connected to the center tap. The voltage at ILIM is proportional to the current-limit threshold. See the *Setting the Current-Limit* section for more details.

The current-limit circuitry terminates the DH_ on-time immediately when the current-sense voltage (V_{CS_+} - V_{CS_-}) exceeds the current-limit threshold, allowing the output inductor current to ramp down. At the next switching cycle, the PWM pulse is skipped if the output inductor current is still above the current-limit threshold. Otherwise, the new cycle initiates as normal.

The MAX8809A/MAX8810A offer foldback-current protection under soft-start and overload conditions. This feature allows the VRM to safely operate under short-circuit conditions and to automatically recover once the short-circuit condition is removed. If the output voltage falls below the VRREADY threshold during an overcurrent event, the foldback current-limit circuitry sets the current-limit threshold to half the user-selected value.

Output Differential Sensing (RS+, RS-)

The MAX8809A/MAX8810A feature differential output-voltage sensing to achieve the highest possible output accuracy. This allows the controllers to sense the actual voltage at the load, so the controller can compensate for losses in the power output and ground lines. Traces from the load point back to RS+ and RS- should be routed close to each other and as far away as possible from noise sources (such as inductors and high di/dt traces). Use a ground plane to shield the remote-sense traces from noise sources. To filter out common-mode noise, RC filtering is recommended for these inputs as shown in Figure 5. For VRD applications, a 100Ω resistor with a 1nF capacitor should be used. For VRM applications, additional 50Ω resistors should be connected from these inputs to the local outputs of the converter before the VRM connector. This avoids excessive voltage at the CPU in case the remote-sense connections get disconnected.

Programming the Output-Voltage Droop

Both the MAX8809A and MAX8810A employ peak-current-mode control with finite gain to actively set the output-voltage droop. Figure 6 shows the simplified control block diagram. The relationship between the output inductor current in an N-phase DC-DC converter and the output voltage of the voltage-error amplifier is:

$$V_C = \frac{I_{OUT}}{N} \times R_{SENSE} \times G_{CA}$$

where G_{CA} (30V/V typ) is the gain of the differential current amplifier and N is the number of phases. I_{OUT} is the total output current. Therefore, when the output current increases, V_C increases. On the other hand, V_C is related to the output voltage of the converter by the following equation:

$$V_C = g_{MV} \times R_{COMP} \times (V_{DAC} - V_{OUT})$$

where g_{MV} is the transconductance of the voltage-error amplifier (2mS typ) and V_{DAC} is the VID-generated voltage.

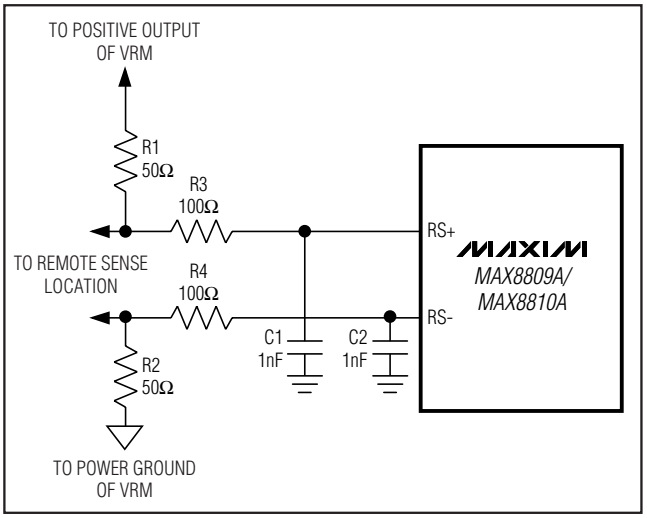

Figure 5. Recommended Filtering for Output-Voltage Remote Sensing

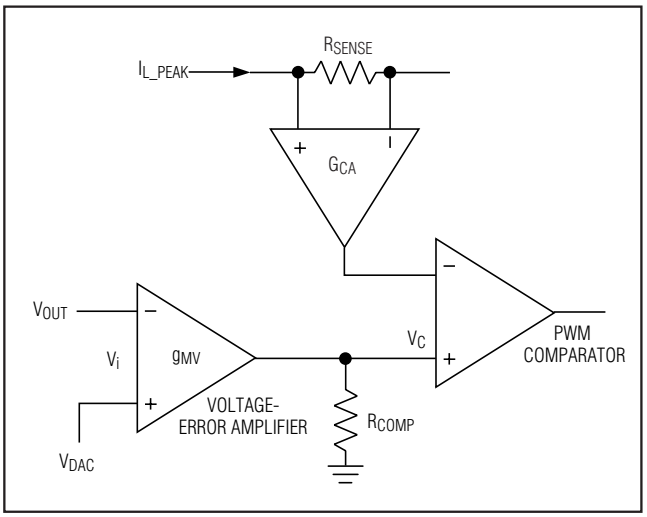

Figure 6. Simplified Peak Current-Mode Control IC with Active Output-Voltage Positioning

The DC gain of the voltage-error amplifier is equal to $g_{MV} \times R_{COMP}$. From the previous equations it is clear that the output-voltage droop can be accurately programmed if the DC gain of the voltage-error amplifier is set to be a finite value. As the output current increases, V_C increases and, consequently, V_{OUT} decreases. Define the output-droop resistance, R_{DROOP}, as:

$$R_{DROOP} = \frac{(V_{DAC} - V_{OUT})}{I_{OUT}}$$

then R_{DROOP} can be expressed as:

$$R_{DROOP} = \frac{R_{SENSE} \times G_{CA}}{N \times g_{MV} \times R_{COMP}}$$

Since G_{CA} and g_{MV} are constants, R_{DROOP} is solely determined by R_{COMP} when R_{SENSE} and N are chosen.

Peak current-mode control with finite gain is the simplest way to achieve the output-voltage droop without introducing a separate current loop, which is the case for voltage-mode control. Therefore, the response time of the output-voltage droop is the same as the voltage-feedback loop, resulting in fast output-voltage-droop transient response and less output capacitance than solutions using voltage-mode control.

Other features offered by peak-current-mode control are excellent line regulation and inherent current sharing between phases. Standard peak-current-mode control does have one disadvantage in that current matching between phases is impacted by the inductor mismatch (tolerance) between phases. Because only the current peak is controlled, any mismatch in the inductor value between two phases creates an inductor ripple current mismatch, which, in turn, creates a DC current mismatch between those two phases. Tolerance mismatch between the current-sense capacitors used in DCR current sensing creates the exact same DC current mismatch as an inductor mismatch.

Maxim's proprietary RA^2 technology addresses this issue by averaging out the inductor ripple current individually at each phase, as shown in Figure 7. The rapid active average circuitry learns the peak-to-peak ripple current of each phase in 5 to 10 switching cycles and then biases the peak current signal down by half of the peak-to-peak ripple current, consequently eliminating the impact of both output inductance and DCR current-sense capacitance variations. Since the rapid active average circuitry is not part of the current-loop path, it does not slow down the transient response.

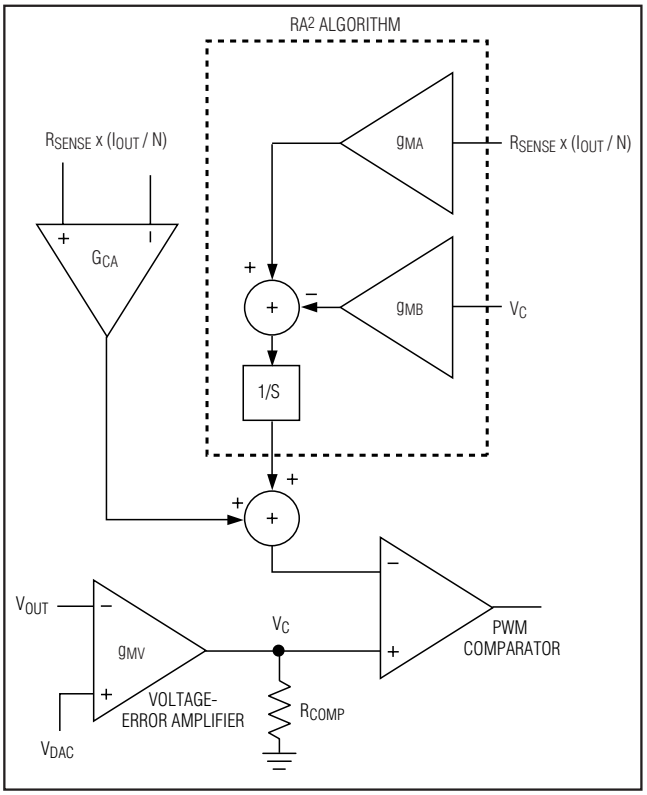

Figure 7. Implementation of the Rapid Active Averaging (RA^2) Algorithm

Programming the Output Offset Voltage

According to the Intel VRD specifications, the output voltage at no load cannot exceed the voltage specified by the VID code, including the initial set tolerance, ripple voltage, and other errors. Therefore, the actual output voltage should be biased lower to compensate for these errors. For the MAX8809A, the output-voltage offset is created through a resistor-divider that is connected between REF and GND, with the center tap connected to COMP as shown in Figure 8. This resistor-divider also sets the output load-line. The MAX8810A contains a BUF output that makes the output-voltage offset setting independent of the output load-line. To program the output-voltage offset, connect a resistor between COMP and GND. A resistor between BUF and COMP sets the output load-line. See the *Loop Compensation Design* section for details on setting the output-voltage offset.

VRD11/VRD10, K8 Rev F 2/3/4-Phase PWM Controllers with Integrated Dual MOSFET Drivers

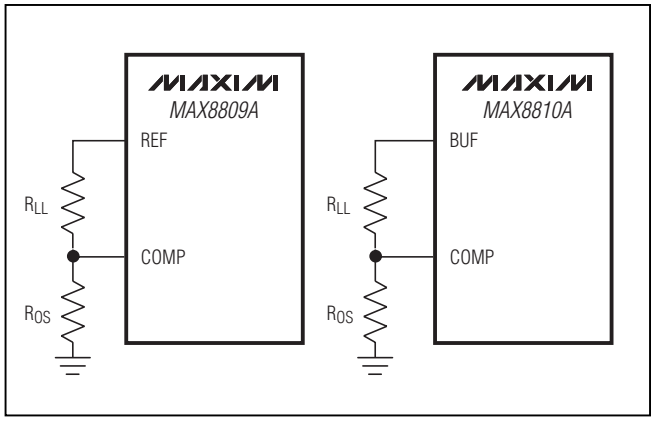

Figure 8. Programming the Output Offset Voltage

Load-Line Independent Inductor DC Resistance Temperature Compensation

Changes in inductor resistance due to temperature cause a change in the output-droop characteristic. This is compensated by changing the gain of the current-sense amplifier as a function of temperature. In doing so, the voltage at COMP is independent of temperature, resulting in a temperature-independent load-line setting. Additionally, the output short-circuit protection is also temperature independent because current limit is implemented by clamping the voltage at COMP. This technology uses an NTC thermistor solely for temperature compensation, freeing it from being one of the components that determines the output load-line. Therefore, only one NTC thermistor is needed to enable any output load-line. The same NTC thermistor is used for temperature sense for the VRHOT output. The MAX8809A/MAX8810A temperature-compensation scheme is optimized for use with a Panasonic ERTJ1VR103 10kΩ NTC thermistor. Other thermistors may be used. Contact your local Maxim representative for more details.

Loop Compensation

During a load transient, the output voltage instantly changes due to the ESR of the output capacitors by an amount equal to their ESR times the change in load current ($\Delta V_{OUT} = R_{ESR} \times \Delta I_{LOAD}$). The output voltage then deviates further based on the speed at which the loop compensates for the load transient. The voltage-positioning method allows better utilization of the output regulation window, resulting in less required output capacitors. The RA^2 architecture adjusts the output current based on the instantaneous output voltage, resulting in fast voltage positioning. The voltage-error amplifier consists of a high-bandwidth, high-accuracy transconductance amplifier (g_{MV} in Figure 7*)*. The negative input of the transconductance amplifier is connected to the output of the remote-voltage differential amplifier, and the positive input is connected to the output of an internal DAC controlled by the VID inputs. The DC gain of the transconductance amplifier is set to a finite value to achieve fast output-voltage positioning by connecting an RC circuit (R_{COMP} and C_{COMP}) from COMP to GND. See the *Loop-Compensation Design* section for details on selecting the required components.

VR Ready Output (VRREADY)

VRREADY is an open-drain output that turns high impedance when the output voltage reaches regulation. VRREADY goes low if V_{OUT} is less than (V_{DAC} - 225mV) or greater than (V_{DAC} + 175mV), signaling an out-of-regulation fault. VRREADY is held low in shutdown, if V_{CC} is less than the UVLO threshold, or during soft-start. For logic-level output voltages, connect an external pullup resistor between VRREADY and the logic power supply. A 100kΩ resistor works well in most applications.

Dynamic VID Change

The MAX8809A/MAX8810A provide the ability for the CPU to dynamically change the VID inputs while the controller is operating (on-the-fly or OTF). The output voltage changes in 6.25mV steps (Intel) or 12.5mV/25mV steps (AMD) when a VID change is detected.

The controller provides a 400ns logic-skew window to prevent false code changes. The controller accepts both step-by-step changes of VID inputs or all-at-once VID input changes. For all-at-once VID input changes, the output-voltage slew rate is the same, 1 LSB per step and 2µs duration. VRREADY is blanked during dynamic VID changes.

Multiphase Operation Selection

The MAX8809A operates in either a 2- or 3-phase configuration. Connect PWM3 to V_{CC} for 2-phase operation.

The MAX8810A operates in 2-, 3- or 4-phase configuration. Connect PWM4 to V_{CC} for 3-phase operation. Connect PWM4 and PWM3 to V_{CC} for 2-phase operation. All active PWM outputs are held low during shutdown.

UVLO and Output Enable

When the IC supply voltage (V_{CC}) is less than the UVLO threshold (4.25V typ), all active PWM outputs are internally pulled low and most internal circuitry is shut down to reduce the quiescent current. When EN is released and V_{CC} > UVLO, the internal 100kΩ resistor pulls EN to V_{CC} and soft-start is initiated (after a typical 2.2ms delay).

When the driver supply voltage ($V_{VL\_}$) is less than its UVLO threshold (3.55V typ), DH_ and DL_ are held low. If $V_{VL\_}$ is above the UVLO threshold and while EN is low, DL_ is driven high and DH_ is held low. This prevents the output of the converter from rising before a valid EN high signal is present.

Soft-Start

The MAX8809A/MAX8810A soft-start with 6.25mV steps, regardless of processor architecture. Connect a resistor between SS/OVP and GND to program the soft-start time. When the device is enabled, SS/OVP is driven to 2V and the current drawn by the set resistor is measured. This current sets the internal delay time between the DAC voltage steps. Select a resistor between 12kΩ and 90.9kΩ for a corresponding soft-start time of 500µs to 6.5ms. For Intel designs, the resistor value is calculated as:

$$R_{SS/OVP}(k\Omega) = \frac{t_{SS} - 0.0183}{0.0532}$$

where t_{SS} is the desired soft-start time (in ms) to the 1.1V V_{BOOT} level. Figure 9 shows the Intel startup sequence, and Table 1 shows the values of the time delays.

For AMD applications, the controllers soft-start up to the voltage set by the VID inputs. The soft-start time is set by the following equation:

$$R_{SS/OVP}(k\Omega) = \frac{t_{SS} - 0.0183}{0.0532} \times \frac{1.1V}{V_{DAC}}$$

where V_{DAC} is the output voltage set by the VID inputs. Figure 10 shows the AMD startup sequence, and Table 2 shows the values of the time delays.

Soft-Stop

When EN goes low, the output of the converter ramps down to 0V in 6.25mV DAC steps in the time set by the SS/OVP input. Once the output reaches 0V, DL is held high and DH is held low to maintain the 0V output. This

Table 1. Intel Startup Sequence Specifications

PARAMETER	MIN	MAX
TD1	1ms	5ms
TD2	50µs	5ms
TD3	50µs	3ms
TD4	—	2.5ms
TD5	50µs	3ms

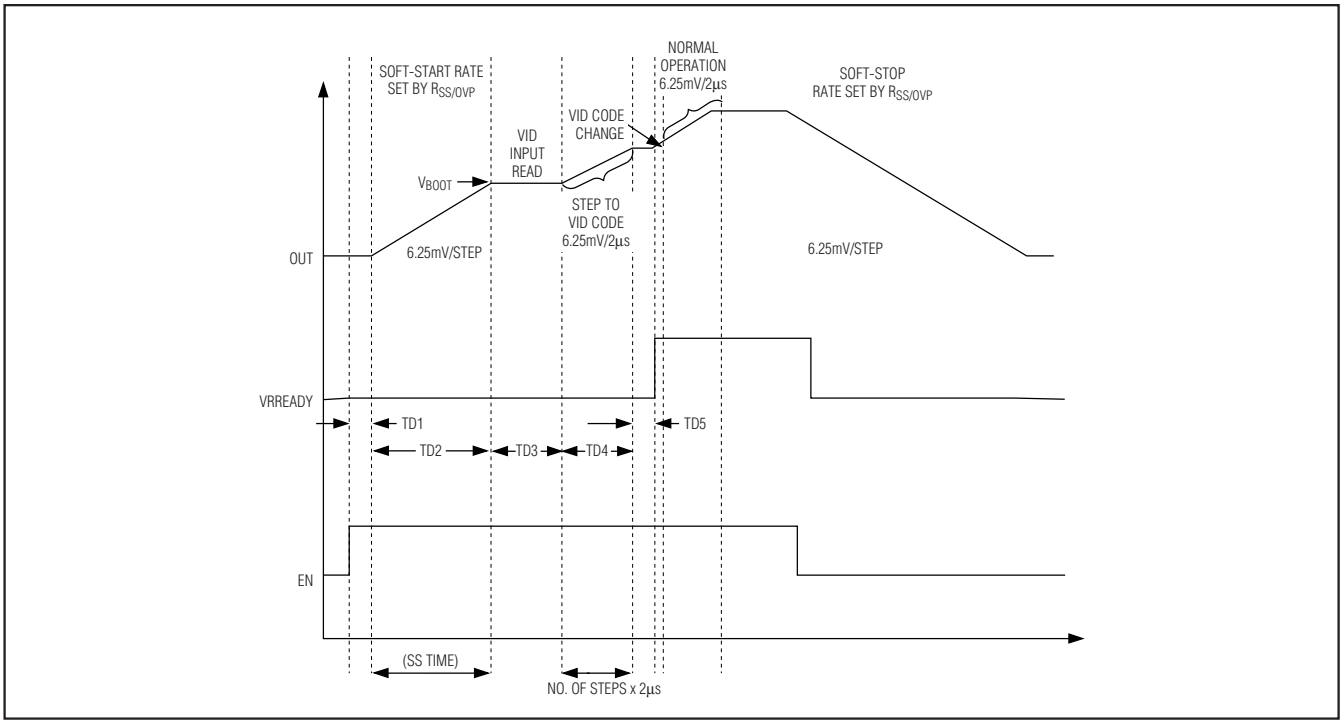

Figure 9. Intel VRD11/VRD10 Startup Sequence

VRD11/VRD10, K8 Rev F 2/3/4-Phase PWM Controllers with Integrated Dual MOSFET Drivers

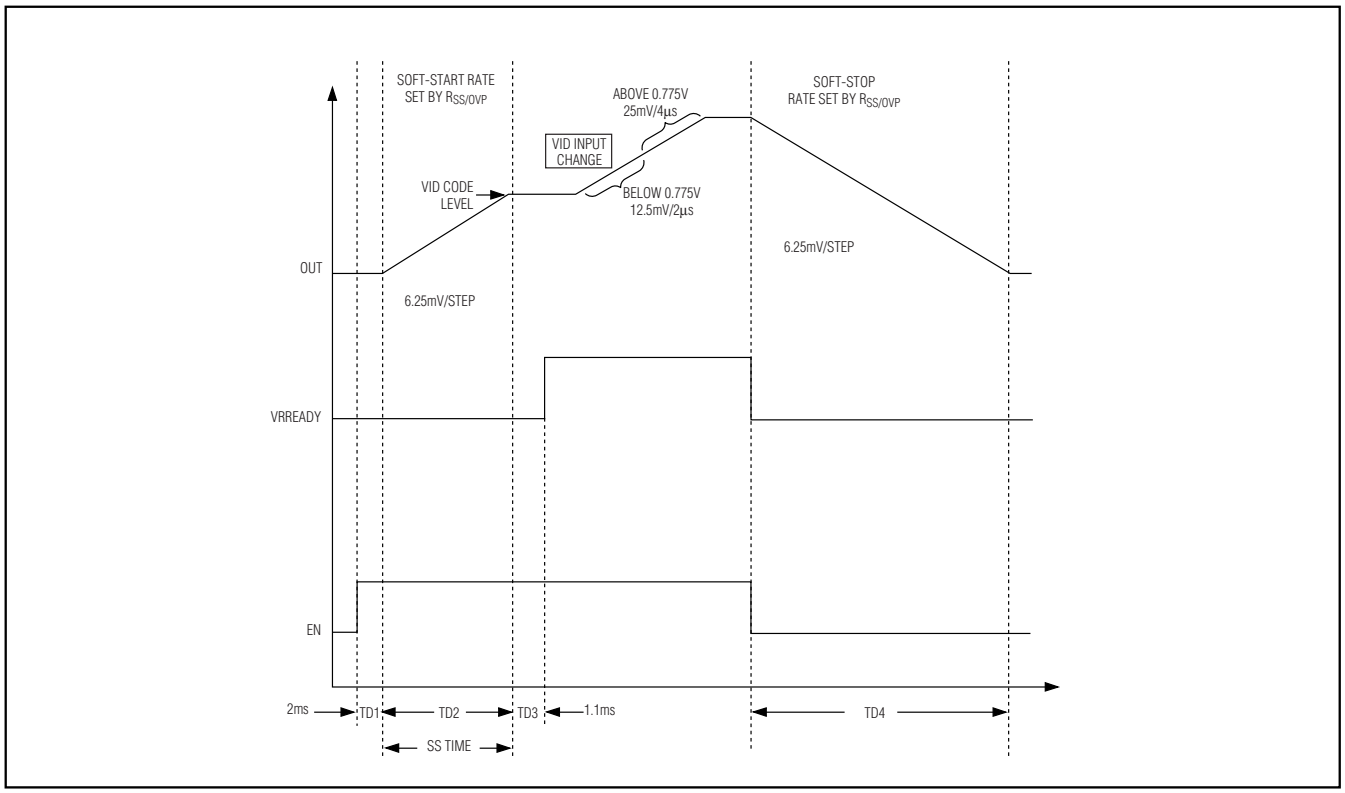

Figure 10. K8 Rev F Startup Sequencing and Timing

Table 2. AMD Startup Sequence Specifications

PARAMETER	MINIMUM TIME (µs)	MAXIMUM TIME (ms)
TD1	1	—
TD2*	500	6.5
TD3	—	20
TD4	—	500

**User programmable.*

approach prevents large negative voltages on the output during shutdown and therefore eliminates the need for a Schottky clamp diode on the output.

Output Overvoltage Protection (OVP)

When the output voltage exceeds the regulation voltage by 200mV (Intel) or exceeds 1.8V (AMD), all active PWM outputs are pulled low and the controller is latched off. SS/OVP is internally pulled to V_{CC} to signal an overvoltage fault. All DH_ outputs are held low and all DL_ outputs are held high to discharge the output. The latch condition can only be cleared by cycling the input voltage (V_{CC}).

Integrated Dual-MOSFET Driver

The MAX8809A/MAX8810A contain a dual-phase gate driver capable of driving 3000pF capacitive loads with only 32ns propagation delay and 11ns typical rise and fall times, allowing operation up to 1.2MHz per phase. Adaptive dead time controls low-side MOSFET turn-on and high-side MOSFET turn-on. This maximizes converter efficiency, while allowing operation with a variety of MOSFETs. A UVLO circuit ensures proper power-on sequencing.

Adaptive Shoot-Through Protection

Adaptive shoot-through protection is incorporated for the switching transition after the high-side MOSFET is turned off and before the low-side MOSFET is turned on. The low-side driver is turned on only when the LX_ voltage falls below 2.5V typical. In addition, a fixed 35ns delay time between the low-side MOSFET turn-off and high-side MOSFET turn-on adds further protection from “shoot-through.” The 35ns time begins after DL_ has fallen through 1.5V typical.

MOSFET Driver UVLO

When V_{VL12} (MAX8809A) or V_{VL1} (MAX8810A) is below the UVLO threshold (3.55 typ), DH_ and DL_ are held

low. Once $V_{VL\_}$ is above the UVLO threshold and EN is low, DL_ is kept high and DH_ is kept low. This prevents the output from rising before a valid EN signal is given.

Boost Circuit for High-Side MOSFET Driver

The gate-drive voltage for the high-side MOSFET drivers is generated by a flying-capacitor boost circuit. The capacitor between BST_ and LX_ is charged from the VL_ supply through an internal switch while the low-side MOSFET is on. When the low-side MOSFET is switched off, the stored voltage on the capacitor is stacked above LX_ to provide the necessary turn-on voltage for the high-side MOSFET(s). No external boost diode is needed. See the *Boost Capacitor Selection* section for details on selecting the correct capacitor.

Thermal Protection

The MAX8809A/MAX8810A feature a thermal-fault-protection circuit. When the junction temperature rises above +160°C typical, an internal thermal sensor activates the shutdown circuit to hold all MOSFET drivers and active PWM outputs low to disable switching. The thermal sensor reactivates the controller after the junction temperature cools by 25°C typical.

Temperature Monitoring (VRTSET, VRHOT)

The MAX8809A/MAX8810A contain temperature-monitoring circuitry that allows the user to program a temperature trip point between +60°C and +125°C, and monitor an active-high, open-drain VRHOT output. Connect a resistor from VRTSET to GND to set the temperature-monitoring threshold. The resistor is calculated as follows:

$$R_{VRTSET} = \frac{800}{0.6K_T} \text{ in k}\Omega$$

where K_T is a temperature scale factor specifically for the Panasonic ERTJ1VR103 NTC thermistor. Table 3 provides values of K_T and the closest standard 1% R_{VRTSET} values needed to program the VRHOT threshold over a +60°C to +125°C range. R_{VRTSET} must be greater than 20kΩ. Contact your local Maxim representative for information on using other thermistors.

Table 3. Temperature Scale Factor

TEMPERATURE (°C)	K_T	R_{VRTSET} (kΩ)
+60	4.497	294
+65	5.453	243
+70	6.580	200
+75	7.903	169
+80	9.447	140
+85	11.244	118
+90	13.325	100
+95	15.725	84.5
+100	18.484	71.5
+105	21.643	61.9
+110	25.247	52.3
+115	29.345	45.3
+120	33.988	39.2
+125	39.231	34

Architecture Selection and Timing

AMD K8 Rev F

The AMD K8 Rev F processor uses a 6-bit VID code that specifies a 0.375V to 1.55V output voltage range (see Table 4). Leave SEL unconnected to select the AMD K8 Rev F architecture. The startup sequencing and timing specifications are shown in Figure 10. Note that the VID input defines the AMD processor boot level, and there is no internal default. The boot level is not latched; therefore, if the codes change during soft-start, the boot level also changes.

Extended Intel VRD10

The Intel VRD10 processor uses a 7-bit VID code that specifies a 0.83125V to 1.6V output voltage range (see Table 5). Connect SEL to GND to select the VRD10 architecture. The startup sequencing and timing specifications are shown in Figure 9. The Intel boot level is internally set to 1.1V; therefore, the VID inputs are ignored during soft-start. In compliance with the Intel VRD specifications, there is a typical 2.2ms delay after EN is asserted before soft-start begins. This delay is not included in the soft-start time set by SS/OVP.

Intel VRD11

The Intel VRD11 processor uses an 8-bit VID code that specifies a 0.3125V to 1.6V output voltage range (see Table 6). Connect SEL to V_{CC} to select the VRD11 architecture. The startup sequencing and timing specifications are shown in Figure 9. The Intel boot level is internally set to 1.1V; therefore, the VID inputs are ignored during soft-start. In compliance with the Intel VRD specifications, there is a typical 2.2ms delay after EN is asserted before soft-start begins. This delay is not included in the soft-start time set by SS/OVP.

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Table 4. AMD K8 Rev F VID Code, SEL = UNCONNECTED

VID5	VID4	VID3	VID2	VID1	VID0	V_{OUT} (V)
1	1	1	1	1	1	0.3750
1	1	1	1	1	0	0.3875
1	1	1	1	0	1	0.4000
1	1	1	1	0	0	0.4125
1	1	1	0	1	1	0.4250
1	1	1	0	1	0	0.4375
1	1	1	0	0	1	0.4500
1	1	1	0	0	0	0.4625
1	1	0	1	1	1	0.4750
1	1	0	1	1	0	0.4875
1	1	0	1	0	1	0.5000
1	1	0	1	0	0	0.5125
1	1	0	0	1	1	0.5250
1	1	0	0	1	0	0.5375
1	1	0	0	0	1	0.5500
1	1	0	0	0	0	0.5625
1	0	1	1	1	1	0.5750
1	0	1	1	1	0	0.5875
1	0	1	1	0	1	0.6000
1	0	1	1	0	0	0.6125
1	0	1	0	1	1	0.6250
1	0	1	0	1	0	0.6375
1	0	1	0	0	1	0.6500
1	0	1	0	0	0	0.6625
1	0	0	1	1	1	0.6750
1	0	0	1	1	0	0.6875
1	0	0	1	0	1	0.7000
1	0	0	1	0	0	0.7125
1	0	0	0	1	1	0.7250
1	0	0	0	1	0	0.7375
1	0	0	0	0	1	0.7500
1	0	0	0	0	0	0.7625

VID5	VID4	VID3	VID2	VID1	VID0	V_{OUT} (V)
0	1	1	1	1	1	0.7750
0	1	1	1	1	0	0.8000
0	1	1	1	0	1	0.8250
0	1	1	1	0	0	0.8500
0	1	1	0	1	1	0.8750
0	1	1	0	1	0	0.9000
0	1	1	0	0	1	0.9250
0	1	1	0	0	0	0.9500
0	1	0	1	1	1	0.9750
0	1	0	1	1	0	1.0000
0	1	0	1	0	1	1.0250
0	1	0	1	0	0	1.0500
0	1	0	0	1	1	1.0750
0	1	0	0	1	0	1.1000
0	1	0	0	0	1	1.1250
0	1	0	0	0	0	1.1500
0	0	1	1	1	1	1.1750
0	0	1	1	1	0	1.2000
0	0	1	1	0	1	1.2250
0	0	1	1	0	0	1.2500
0	0	1	0	1	1	1.2750
0	0	1	0	1	0	1.3000
0	0	1	0	0	1	1.3250
0	0	1	0	0	0	1.3500
0	0	0	1	1	1	1.3750
0	0	0	1	1	0	1.4000
0	0	0	1	0	1	1.4250
0	0	0	1	0	0	1.4500
0	0	0	0	1	1	1.4750
0	0	0	0	1	0	1.5000
0	0	0	0	0	1	1.5250
0	0	0	0	0	0	1.5500

Note: *VID voltage increment is 12.5mV from 0.3875 to 0.775 and 25mV from 0.775 to 1.550.*

Table 5. Extended Intel VRD10 VID Code, SEL = GND

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{OUT} (V)
1	1	0	1	0	1	0	1.60000
0	1	0	1	0	1	0	1.59375
1	0	0	1	0	1	1	1.58750
0	0	0	1	0	1	1	1.58125
1	1	0	1	0	1	1	1.57500
0	1	0	1	0	1	1	1.56875
1	0	0	1	1	0	0	1.56250
0	0	0	1	1	0	0	1.55625
1	1	0	1	1	0	0	1.55000
0	1	0	1	1	0	0	1.54375
1	0	0	1	1	0	1	1.53750
0	0	0	1	1	0	1	1.53125
1	1	0	1	1	0	1	1.52500
0	1	0	1	1	0	1	1.51875
1	0	0	1	1	1	0	1.51250
0	0	0	1	1	1	0	1.50625
1	1	0	1	1	1	0	1.50000
0	1	0	1	1	1	0	1.49375
1	0	0	1	1	1	1	1.48750
0	0	0	1	1	1	1	1.48125
1	1	0	1	1	1	1	1.47500
0	1	0	1	1	1	1	1.46875
1	0	1	0	0	0	0	1.46250
0	0	1	0	0	0	0	1.45625
1	1	1	0	0	0	0	1.45000
0	1	1	0	0	0	0	1.44375
1	0	1	0	0	0	1	1.43750
0	0	1	0	0	0	1	1.43125
1	1	1	0	0	0	1	1.42500
0	1	1	0	0	0	1	1.41875
1	0	1	0	0	1	0	1.41250
0	0	1	0	0	1	0	1.40625

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{OUT} (V)
1	1	1	0	0	1	0	1.40000
0	1	1	0	0	1	0	1.39375
1	0	1	0	0	1	1	1.38750
0	0	1	0	0	1	1	1.38125
1	1	1	0	0	1	1	1.37500
0	1	1	0	0	1	1	1.36875
1	0	1	0	1	0	0	1.36250
0	0	1	0	1	0	0	1.35625
1	1	1	0	1	0	0	1.35000
0	1	1	0	1	0	0	1.34375
1	0	1	0	1	0	1	1.33750
0	0	1	0	1	0	1	1.33125
1	1	1	0	1	0	1	1.32500
0	1	1	0	1	0	1	1.31875
1	0	1	0	1	1	0	1.31250
0	0	1	0	1	1	0	1.30625
1	1	1	0	1	1	0	1.30000
0	1	1	0	1	1	0	1.29375
1	0	1	0	1	1	1	1.28750
0	0	1	0	1	1	1	1.28125
1	1	1	0	1	1	1	1.27500
0	1	1	0	1	1	1	1.26875
1	0	1	1	0	0	0	1.26250
0	0	1	1	0	0	0	1.25625
1	1	1	1	0	0	0	1.25000
0	1	1	1	0	0	0	1.24375
1	0	1	1	0	0	1	1.23750
0	0	1	1	0	0	1	1.23125
1	1	1	1	0	0	1	1.22500
0	1	1	1	0	0	1	1.21875
1	0	1	1	0	1	0	1.21250
0	0	1	1	0	1	0	1.20625

VRD11/VRD10, K8 Rev F 2/3/4-Phase PWM Controllers with Integrated Dual MOSFET Drivers

Table 5. Extended Intel VRD10 VID Code, SEL = GND (continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{OUT} (V)
1	1	1	1	0	1	0	1.20000
0	1	1	1	0	1	0	1.19375
1	0	1	1	0	1	1	1.18750
0	0	1	1	0	1	1	1.18125
1	1	1	1	0	1	1	1.17500
0	1	1	1	0	1	1	1.16875
1	0	1	1	1	0	0	1.16250
0	0	1	1	1	0	0	1.15625
1	1	1	1	1	0	0	1.15000
0	1	1	1	1	0	0	1.14375
1	0	1	1	1	0	1	1.13750
0	0	1	1	1	0	1	1.13125
1	1	1	1	1	0	1	1.12500
0	1	1	1	1	0	1	1.11875
1	0	1	1	1	1	0	1.11250
0	0	1	1	1	1	0	1.10625
1	1	1	1	1	1	0	1.10000
0	1	1	1	1	1	0	1.09375
1	0	1	1	1	1	1	OFF
0	0	1	1	1	1	1	OFF
1	1	1	1	1	1	1	OFF
0	1	1	1	1	1	1	OFF
1	0	0	0	0	0	0	1.08750
0	0	0	0	0	0	0	1.08125
1	1	0	0	0	0	0	1.07500
0	1	0	0	0	0	0	1.06875
1	0	0	0	0	0	1	1.06250
0	0	0	0	0	0	1	1.05625
1	1	0	0	0	0	1	1.05000
0	1	0	0	0	0	1	1.04375
1	0	0	0	0	1	0	1.03750
0	0	0	0	0	1	0	1.03125

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{OUT} (V)
1	1	0	0	0	1	0	1.02500
0	1	0	0	0	1	0	1.01875
1	0	0	0	0	1	1	1.01250
0	0	0	0	0	1	1	1.00625
1	1	0	0	0	1	1	1.00000
0	1	0	0	0	1	1	0.99375
1	0	0	0	1	0	0	0.98750
0	0	0	0	1	0	0	0.98125
1	1	0	0	1	0	0	0.97500
0	1	0	0	1	0	0	0.96875
1	0	0	0	1	0	1	0.96250
0	0	0	0	1	0	1	0.95625
1	1	0	0	1	0	1	0.95000
0	1	0	0	1	0	1	0.94375
1	0	0	0	1	1	0	0.93750
0	0	0	0	1	1	0	0.93125
1	1	0	0	1	1	0	0.92500
0	1	0	0	1	1	0	0.91875
1	0	0	0	1	1	1	0.91250
0	0	0	0	1	1	1	0.90625
1	1	0	0	1	1	1	0.90000
0	1	0	0	1	1	1	0.89375
1	0	0	1	0	0	0	0.88750
0	0	0	1	0	0	0	0.88125
1	1	0	1	0	0	0	0.87500
0	1	0	1	0	0	0	0.86875
1	0	0	1	0	0	1	0.86250
0	0	0	1	0	0	1	0.85625
1	1	0	1	0	0	1	0.85000
0	1	0	1	0	0	1	0.84375
1	0	0	1	0	1	0	0.83750
0	0	0	1	0	1	0	0.83125

Table 6. Intel VRD11 VID Code, SEL = V_{CC}

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{OUT} (V)
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	OFF
0	0	0	0	0	0	1	0	1.60000
0	0	0	0	0	0	1	1	1.59375
0	0	0	0	0	1	0	0	1.58750
0	0	0	0	0	1	0	1	1.58125
0	0	0	0	0	1	1	0	1.57500
0	0	0	0	0	1	1	1	1.56875
0	0	0	0	1	0	0	0	1.56250
0	0	0	0	1	0	0	1	1.55625
0	0	0	0	1	0	1	0	1.55000
0	0	0	0	1	0	1	1	1.54375
0	0	0	0	1	1	0	0	1.53750
0	0	0	0	1	1	0	1	1.53125
0	0	0	0	1	1	1	0	1.52500
0	0	0	0	1	1	1	1	1.51875
0	0	0	1	0	0	0	0	1.51250
0	0	0	1	0	0	0	1	1.50625
0	0	0	1	0	0	1	0	1.50000
0	0	0	1	0	0	1	1	1.49375
0	0	0	1	0	1	0	0	1.48750
0	0	0	1	0	1	0	1	1.48125
0	0	0	1	0	1	1	0	1.47500
0	0	0	1	0	1	1	1	1.46875
0	0	0	1	1	0	0	0	1.46250
0	0	0	1	1	0	0	1	1.45625
0	0	0	1	1	0	1	0	1.45000
0	0	0	1	1	0	1	1	1.44375
0	0	0	1	1	1	0	0	1.43750
0	0	0	1	1	1	0	1	1.43125
0	0	0	1	1	1	1	0	1.42500
0	0	0	1	1	1	1	1	1.41875
0	0	1	0	0	0	0	0	1.41250
0	0	1	0	0	0	0	1	1.40625
0	0	1	0	0	0	1	0	1.40000
0	0	1	0	0	0	1	1	1.39375
0	0	1	0	0	1	0	0	1.38750
0	0	1	0	0	1	0	1	1.38125
0	0	1	0	0	1	1	0	1.37500
0	0	1	0	0	1	1	1	1.36875

Table 6. Intel VRD11 VID Code, SEL = V_{CC} (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{OUT} (V)
0	0	1	0	1	0	0	0	1.36250
0	0	1	0	1	0	0	1	1.35625
0	0	1	0	1	0	1	0	1.35000
0	0	1	0	1	0	1	1	1.34375
0	0	1	0	1	1	0	0	1.33750
0	0	1	0	1	1	0	1	1.33125
0	0	1	0	1	1	1	0	1.32500
0	0	1	0	1	1	1	1	1.31875
0	0	1	1	0	0	0	0	1.31250
0	0	1	1	0	0	0	1	1.30625
0	0	1	1	0	0	1	0	1.30000
0	0	1	1	0	0	1	1	1.29375
0	0	1	1	0	1	0	0	1.28750
0	0	1	1	0	1	0	1	1.28125
0	0	1	1	0	1	1	0	1.27500
0	0	1	1	0	1	1	1	1.26875
0	0	1	1	1	0	0	0	1.26250
0	0	1	1	1	0	0	1	1.25625
0	0	1	1	1	0	1	0	1.25000
0	0	1	1	1	0	1	1	1.24375
0	0	1	1	1	1	0	0	1.23750
0	0	1	1	1	1	0	1	1.23125
0	0	1	1	1	1	1	0	1.22500
0	0	1	1	1	1	1	1	1.21875
0	1	0	0	0	0	0	0	1.21250
0	1	0	0	0	0	0	1	1.20625
0	1	0	0	0	0	1	0	1.20000
0	1	0	0	0	0	1	1	1.19375
0	1	0	0	0	1	0	0	1.18750
0	1	0	0	0	1	0	1	1.18125
0	1	0	0	0	1	1	0	1.17500
0	1	0	0	0	1	1	1	1.16875
0	1	0	0	1	0	0	0	1.16250
0	1	0	0	1	0	0	1	1.15625
0	1	0	0	1	0	1	0	1.15000
0	1	0	0	1	0	1	1	1.14375
0	1	0	0	1	1	0	0	1.13750
0	1	0	0	1	1	0	1	1.13125
0	1	0	0	1	1	1	0	1.12500
0	1	0	0	1	1	1	1	1.11875

Table 6. Intel VRD11 VID Code, SEL = V_{CC} (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{OUT} (V)
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625
0	1	0	1	0	0	1	0	1.10000
0	1	0	1	0	0	1	1	1.09375
0	1	0	1	0	1	0	0	1.08750
0	1	0	1	0	1	0	1	1.08125
0	1	0	1	0	1	1	0	1.07500
0	1	0	1	0	1	1	1	1.06875
0	1	0	1	1	0	0	0	1.06250
0	1	0	1	1	0	0	1	1.05625
0	1	0	1	1	0	1	0	1.05000
0	1	0	1	1	0	1	1	1.04375
0	1	0	1	1	1	0	0	1.03750
0	1	0	1	1	1	0	1	1.03125
0	1	0	1	1	1	1	0	1.02500
0	1	0	1	1	1	1	1	1.01875
0	1	1	0	0	0	0	0	1.01250
0	1	1	0	0	0	0	1	1.00625
0	1	1	0	0	0	1	0	1.00000
0	1	1	0	0	0	1	1	0.99375
0	1	1	0	0	1	0	0	0.98750
0	1	1	0	0	1	0	1	0.98125
0	1	1	0	0	1	1	0	0.97500
0	1	1	0	0	1	1	1	0.96875
0	1	1	0	1	0	0	0	0.96250
0	1	1	0	1	0	0	1	0.95625
0	1	1	0	1	0	1	0	0.95000
0	1	1	0	1	0	1	1	0.94375
0	1	1	0	1	1	0	0	0.93750
0	1	1	0	1	1	0	1	0.93125
0	1	1	0	1	1	1	0	0.92500
0	1	1	0	1	1	1	1	0.91875
0	1	1	1	0	0	0	0	0.91250
0	1	1	1	0	0	0	1	0.90625
0	1	1	1	0	0	1	0	0.90000
0	1	1	1	0	0	1	1	0.89375
0	1	1	1	0	1	0	0	0.88750
0	1	1	1	0	1	0	1	0.88125
0	1	1	1	0	1	1	0	0.87500
0	1	1	1	0	1	1	1	0.86875

Table 6. Intel VRD11 VID Code, SEL = V_{CC} (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{OUT} (V)
0	1	1	1	1	0	0	0	0.86250
0	1	1	1	1	0	0	1	0.85625
0	1	1	1	1	0	1	0	0.85000
0	1	1	1	1	0	1	1	0.84375
0	1	1	1	1	1	0	0	0.83750
0	1	1	1	1	1	0	1	0.83125
0	1	1	1	1	1	1	0	0.82500
0	1	1	1	1	1	1	1	0.81875
1	0	0	0	0	0	0	0	0.81250
1	0	0	0	0	0	0	1	0.80625
1	0	0	0	0	0	1	0	0.80000
1	0	0	0	0	0	1	1	0.79375
1	0	0	0	0	1	0	0	0.78750
1	0	0	0	0	1	0	1	0.78125
1	0	0	0	0	1	1	0	0.77500
1	0	0	0	0	1	1	1	0.76875
1	0	0	0	1	0	0	0	0.76250
1	0	0	0	1	0	0	1	0.75625
1	0	0	0	1	0	1	0	0.75000
1	0	0	0	1	0	1	1	0.74375
1	0	0	0	1	1	0	0	0.73750
1	0	0	0	1	1	0	1	0.73125
1	0	0	0	1	1	1	0	0.72500
1	0	0	0	1	1	1	1	0.71875
1	0	0	1	0	0	0	0	0.71250
1	0	0	1	0	0	0	1	0.70625
1	0	0	1	0	0	1	0	0.70000
1	0	0	1	0	0	1	1	0.69375
1	0	0	1	0	1	0	0	0.68750
1	0	0	1	0	1	0	1	0.68125
1	0	0	1	0	1	1	0	0.67500
1	0	0	1	0	1	1	1	0.66875
1	0	0	1	1	0	0	0	0.66250
1	0	0	1	1	0	0	1	0.65625
1	0	0	1	1	0	1	0	0.65000
1	0	0	1	1	0	1	1	0.64375
1	0	0	1	1	1	0	0	0.63750
1	0	0	1	1	1	0	1	0.63125
1	0	0	1	1	1	1	0	0.62500
1	0	0	1	1	1	1	1	0.61875

Table 6. Intel VRD11 VID Code, SEL = V_{CC} (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{OUT} (V)
1	0	1	0	0	0	0	0	0.61250
1	0	1	0	0	0	0	1	0.60625
1	0	1	0	0	0	1	0	0.60000
1	0	1	0	0	0	1	1	0.59375
1	0	1	0	0	1	0	0	0.58750
1	0	1	0	0	1	0	1	0.58125
1	0	1	0	0	1	1	0	0.57500
1	0	1	0	0	1	1	1	0.56875
1	0	1	0	1	0	0	0	0.56250
1	0	1	0	1	0	0	1	0.55625
1	0	1	0	1	0	1	0	0.55000
1	0	1	0	1	0	1	1	0.54375
1	0	1	0	1	1	0	0	0.53750
1	0	1	0	1	1	0	1	0.53125
1	0	1	0	1	1	1	0	0.52500
1	0	1	0	1	1	1	1	0.51875
1	0	1	1	0	0	0	0	0.51250
1	0	1	1	0	0	0	1	0.50625
1	0	1	1	0	0	1	0	0.50000
1	1	1	1	1	1	1	0	OFF
1	1	1	1	1	1	1	1	OFF

Design Procedure

The following sections detail the selection process for the external components used with the MAX8809A/MAX8810A. Contact your local Maxim representative to obtain a spreadsheet-based tool to facilitate your design.

Setting the Switching Frequency

The switching frequency influences the switching loss, the size of the power MOSFETs, and the size of power components such as output inductors and capacitors. Higher switching frequencies result in smaller external components and more compact designs. However, power-MOSFET switching losses and magnetic core losses in the output inductor increase with switching frequency, reducing efficiency. Select a switching frequency as a tradeoff between size and efficiency. Once the per-phase switching frequency is selected, the internal oscillator frequency (f_{OSC}) must be set. Determine the required oscillator frequency based on the desired per-phase switching frequency (f_{SW}) from Table 7.

Table 7. Required Clock Frequency for Per-Phase Switching Frequency

NO. OF PHASES	CONFIGURATION	f_{OSC}
2	PWM3 = V_{CC} (MAX8809A); PWM3 = PWM4 = V_{CC} (MAX8810A)	4 x f_{SW}
3	PWM4 = V_{CC} (MAX8810A)	3 x f_{SW}
4	MAX8810A only	4 x f_{SW}

For 2- or 4-phase designs, the internal clock frequency should be set at four times the desired per-phase switching frequency. In 3-phase designs, the internal clock frequency should be set at three times the desired per-phase switching frequency. Set the internal clock frequency with a resistor from OSC to GND (R_{OSC}). The value of R_{OSC} for a given internal clock frequency is approximated from the following equation:

$$R_{OSC} = 161.88 \times f_{OSC}^{-1.2074}$$

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where f_{OSC} is given in MHz and R_{OSC} is in kΩ. Also see the Per-Phase Frequency vs. R_{OSC} graph in the *Typical Operating Characteristics* for the relationship between the clock frequency and the value of the frequency-setting resistor.

Output Inductor Selection

The output inductor is selected based on the desired amount of inductor ripple current. A larger inductance value minimizes output ripple current and increases efficiency but slows down the output-inductor-current slew rate during a load transient. LIR is the ratio of ripple current to the total current per phase. For the best tradeoff of size, cost, and efficiency, an LIR of 30% to 60% is recommended (LIR = 0.3 to 0.6). Choose a higher LIR when more phases are used to take advantage of ripple-current cancellation. The inductor value is determined from:

$$L \geq \frac{V_{OUT} \times (1-D) \times N}{LIR \times f_{SW} \times I_{OUT\_MAX}}$$

where f_{SW} is the per-phase switching frequency, I_{OUT_MAX} is the maximum-rated output current, D is the duty ratio, N is the number of phases, and V_{OUT} is the output voltage at a given VID code. The output-inductor ripple current produces a ripple voltage across the output-capacitor ESR that usually is the dominant component of the output voltage ripple. For an N-phase buck converter with a D x N factor of less than 1, the output ripple voltage, V_{RIPPLE}, can be calculated using:

$$V_{RIPPLE} = \frac{V_{OUT} \times R_{ESR\_CO} \times (1-(D \times N))}{f_{SW} \times L}$$

This equation takes into account the voltage ripple cancellation from multiphase designs. Optimum voltage positioning (droop) requires the effective output-capacitor ESR to match the load resistance, R_O. For initial ripple-voltage estimates, replace R_{ESR_CO} with R_O. If the output-ripple-voltage specification is not satisfied, a larger value of output inductance should be chosen. The selected inductor should have the lowest possible DC resistance, and the saturation current should be greater than the peak inductor current, I_{PEAK}. I_{PEAK} is found from:

$$I_{PEAK} = \frac{I_{OUT\_MAX}}{N} \times \left(1 + \frac{LIR}{2}\right)$$

When the DC resistance (R_{DC}) of the output inductor is used for current sensing, the DC resistance should be a minimum of 0.5mΩ.

It is also important that the peak-to-peak ripple voltage at the input of the current-sense amplifier not exceed 23mV:

$$(V_{CS+} - V_{CS-}) = I_{RIPPLE} \times R_{SENSE}$$

where R_{SENSE} is the sense resistance value at the highest operating temperature. If this condition is not met, then the LIR must be adjusted or the input signal to the current-sense amplifier must be scaled down with a resistor-divider.

Output Capacitor Selection

In most cases, selection of the output capacitor is dictated by the target ESR requirement, $R_{ESR\_CO} = R_O$ (load resistance), to meet the core-supply transient response. However, the minimum output capacitance, $C_{O(MIN)}$, required to meet load-dump requirements, is estimated based on energy balance from:

$$C_{O(MIN)} \geq \frac{1}{2} \times \frac{L \times \left(I_{INIT}^2 - I_{FIN}^2\right)}{N \times \left(V_{FIN} - V_{INIT} + V_{OV}\right) \times V_{INIT}}$$

where I_{INIT} and I_{FIN} are the initial and final values of the inductor current during a load dump, V_{INIT} is the voltage prior to the load dump, V_{FIN} is the voltage after, and V_{OV} is the allowed overshoot above V_{FIN}. The above equation is an approximation, and the output-capacitance value obtained serves as a good starting point. The final value should be obtained from actual measurements.

There is also an upper limit on the amount of output capacitance to meet the OTF VID change requirement. Too much output capacitance can prevent the output voltage from reaching the new VID output voltage within the OTF time window:

$$C_{O(MAX)} \leq \frac{\left(I_{LIM} - I_{OUT\_MAX}\right) \times t_{OTF}}{\Delta V_{OTF}}$$

where t_{OTF} is the time window to achieve ΔV_{OTF} (change in output voltage). If $C_{O(MAX)}$ is less than $C_{O(MIN)}$, the system does not meet the VID OTF specification. I_{LIM} is usually set at 110% to 120% of I_{OUT_MAX}.

RMS ripple current rating is an additional requirement for the output capacitors. For a multiphase buck converter, the RMS ripple current in the output capacitors is given by:

$$I_{CO\_RMS} = \frac{V_{OUT} \times (1-N \times D)}{2\sqrt{3} \times L \times f_{SW}}$$

for (N x D) ≤ 1, where D is the duty cycle and is computed from the following equation:

$$D = \frac{N \times V_{OUT} + I_{OUT\_MAX} \times (R_{DSON\_LS} + R_{DC})}{N \times V_{IN} - I_{OUT\_MAX} \times (R_{DSON\_HS} - R_{DS\_LO})}$$

Use the maximum input voltage for calculating the duty cycle to obtain the worst-case RMS ripple current. R_{DSON_LS} and R_{DSON_HS} are the on-state resistances of the low-side and high-side MOSFETs, respectively, and R_{DC} is the DC resistance of the output inductor.

Input Capacitor Selection

The input capacitor reduces the peak current drawn from the power source and reduces the noise and voltage ripple on the input DC voltage bus caused by the circuit's switching. The input capacitors must meet the ripple-current requirement (I_{RMS}) imposed by the switching currents as defined by the following equation:

$$I_{RMS} = D \times I_{OUT\_MAX} \times \sqrt{\frac{1}{N \times D} - 1}$$

for (D x N) ≤ 1

Use the minimum input voltage for calculating the duty cycle to obtain the worst-case input-capacitor RMS ripple current. Low-ESR aluminum electrolytic, polymer, or ceramic capacitors should be used to avoid large voltage transients at the input during a large step load change at the output. The ripple-current specifications provided by the manufacturer should be carefully reviewed for temperature derating. Additional small-value, low-ESL ceramic capacitors (1µF to 10µF with proper voltage rating) can be used in parallel to reduce any high-frequency ringing.

Boost Capacitor Selection

The MAX8809A/MAX8810A use a bootstrap circuit to generate the floating supply voltages for the high-side drivers. The selected high-side MOSFET determines the appropriate boost capacitance values according to the following equation:

$$C_{BST} = \frac{Q_{GATE\_HS} \times M_{HS}}{\Delta V_{BST}}$$

where M_{HS} is the total number of high-side MOSFETs handled by each BST_ capacitor, Q_{GATE_HS} is the total gate charge of each high-side MOSFET, and ΔV_{BST} is the voltage variation allowed on the high-side MOSFET drive. Choose ΔV_{BST} = 0.1V to 0.2V when determining the $C_{BST\_}$ value. Use low-ESR ceramic capacitors for $C_{BST\_}$. Note that Q_{GATE_HS} is a function of gate-drive voltage $V_{VL\_}$ and should be obtained from the MOSFET data sheet V_{GS} vs. Q_{GATE} curve.

VL_ Bypass Capacitor Selection

VL_ provides the supply voltages for the low-side drivers. The decoupling capacitor at VL_ also charges the high-side driver's BST capacitor during the time period when the low-side MOSFET is turned on. Therefore, the decoupling capacitor for VL_ should be large enough to minimize the ripple voltage during switching transitions. Choose $C_{VL\_}$ according to the following equation:

$$C_{VL\_} = 10 \times C_{BST\_}$$

Power-MOSFET Selection

MOSFET power dissipation depends on the gate-drive voltage (V_D), the on-resistance (R_{DSON}), the total gate charge (Q_{GATE}), and the gate threshold voltage (V_{TH}). The supply voltage (VL_) range for the MOSFET drivers is from 4.5V to 7V. With V_{GATE} < 10V, logic-level threshold MOSFETs are recommended.

Power dissipation in the high-side MOSFET consists of two parts: the conduction loss and the switching loss. The per phase conduction loss for the high side can be calculated from:

$$P_{COND\_HS} = D \times \frac{I^2_{OUT\_MAX}}{N^2} \times (1 + \frac{LIR^2}{12}) \times \frac{R_{DSON\_HS}}{M_{HS}}$$

where N is the number of phases and M_{HS} is the number of MOSFETs in parallel for each phase. Total high-side conduction loss equals the number of phases times P_{COND_HS}.

Switching loss is the major contributor to the high-side MOSFET power dissipation due to the hard switching transition every time it turns on. The switching loss is found from the following:

$$P_{SW\_HS} = \frac{2 \times V_{IN} \times I_{OUT\_MAX}}{N} \times \frac{R_{GATE} \times Q_{MILLER}}{V_D - V_{TH}} \times f_{SW} \times M_{HS}$$

where V_D is the gate-drive voltage and R_{GATE} is the total gate resistance including the driver's on-resistance (see the *Electrical Characteristics* table) and the MOSFET gate resistance. For a logic-level power MOSFET, the gate resistance is approximately 2Ω. Q_{MILLER} is the MOSFET Miller charge found in the MOSFET data sheet. Note that adding more MOSFETs in parallel on the high side increases the switching loss. Smaller Miller gate charge and lower gate resistance usually result in lower switching loss.

The low-side MOSFET power dissipation is mostly attributed to the conduction loss. Switching loss is negligible due to the zero-voltage switching at turn-on and body-diode clamp at turn-off. Power dissipation in the low-side MOSFETs of each phase can be calculated from the following equation:

$$P_{COND\_LS} = (1 - D) \times \frac{I^2_{OUT\_MAX}}{N^2} \times \left(1 + \frac{LIR^2}{12}\right) \times \frac{R_{DSON\_LS}}{M_{LS}}$$

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where M_{LS} is the number of MOSFETs in parallel per phase on the low side. Total power dissipation for the low side equals the number of phases times the low-side conduction loss of each phase.

Even though the switching loss is insignificant in the low-side MOSFETs, R_{DSON} is not the only parameter that should be considered in selecting the low-side MOSFETs. Large Miller capacitance (C_{RSS}) could turn on the low-side MOSFETs momentarily when the drain-to-source voltage goes high at fast slew rates, if the driver cannot hold the gate low. The ratio of C_{RSS}/C_{ISS} should be less than 1/10th for the low-side MOSFETs to avoid shoot-through current due to momentary turn-on of the low-side switch. Adding a resistor between BST_ and $C_{BST\_}$ can slow the high-side MOSFET turn-on. Similarly, adding a capacitor from the gate to the source of the high-side MOSFET has the same effect. However, both methods are at the expense of increasing the high-side switching losses.

Loop-Compensation Design

Loop Compensation with Voltage Positioning

Processor power-supply specifications often require the output voltage to "droop" from its no-load value at a fixed slope with increasing load current. This slope is termed the load-line resistance (R_O). Once the current-sense resistance (R_{SENSE}), the required load-line resistance, and the output offset voltage (V_{OS}) are determined, the values of R_{LL} and R_{OS} (see Figure 8) are calculated from the following equations:

For the MAX8809A:

$$R_{LL} = \frac{1}{\frac{g_{MV}}{2} \times \left(\frac{N \times R_O}{R_{SENSE} \times G_{CA}} - V_{OS} \right)}$$

$$R_{OS} = \frac{1}{\frac{g_{MV}}{2} \times \left(\frac{N \times R_O}{R_{SENSE} \times G_{CA}} + V_{OS} \right) - \frac{1}{20 \times 10^6}}$$

For the MAX8810A:

The 1V BUF output simplifies the R_{OS} calculation considerably. R_{OS} and R_{LL} are calculated as:

$$R_{OS} = \frac{1}{g_{MV} \times V_{OS}}$$

$$R_{LL} = \frac{R_{OS} \times R_{COMP}}{R_{OS} - R_{COMP}}$$

where:

$$R_{COMP} = \frac{R_{SENSE} \times G_{CA}}{N \times g_{MV} \times R_O}$$

The pole due to the load (R_{OUT}) and output capacitance produces a -20dB/decade slope up to the output-capacitor ESR zero frequency. To continue to roll off the gain out to high frequencies at -20dB/decade, the compensation places a pole at the ESR zero frequency. An RC circuit, R_{COMP} and C_{COMP}, must be connected from COMP to ground. Calculate R_{COMP} as the parallel combination of R_{LL} and R_{OS}. The capacitor value can be found from the following equation once the output capacitor ESR is known:

$$C_{COMP} = \frac{R_{ESR\_CO} \times C_O}{R_{COMP}}$$

where R_{ESR_CO} is the total equivalent series resistance and C_O is the total capacitance of the output capacitors.

Loop Compensation with Integral Feedback

For applications that do not implement droop, it is necessary to compensate the loop using integral feedback.

Looking at the transfer function from inductor current $i_L(t)$ to output:

$$G_{VI}(\omega) = R_{OUT} \times \frac{1 + \frac{\omega}{\varpi_{ZERO}}}{1 + \frac{\omega}{\varpi_{POLE}}}$$

The DC gain is the output impedance R_{OUT}:

$$R_{OUT} = V_{OUT} / I_{OUT\_MAX}$$

A pole and zero are present due to the output capacitance (C_O), output-capacitor ESR (R_{ESR_CO}), and the load impedance (R_{OUT}), as follows:

$$\Omega_{POLE} = \frac{1}{(R_{OUT} + R_{ESR\_CO}) \times C_O}$$

and:

$$\Omega_{ZERO} = \frac{1}{\frac{(R_{OUT} \times R_{ESR\_CO})}{(R_{OUT} + R_{ESR\_CO})} \times C_O}$$

The transfer function from control voltage $v_C(t)$ to inductor current $i_L(t)$ is:

$$g_{PWM} = \frac{i_L(t)}{v_C(t)} = \frac{1}{R_{SENSE} \times G_{CA}}$$

where R_{SENSE} is the resistance of the current-sense element, and G_{CA} is the current-sense amplifier gain.

The simplified control-to-output transfer function is then:

$$G_{CONTR\_OUTPUT}(\omega) = g_{PWM} \times G_{VI}(\omega) \times N$$

This simplified transfer function ignores a double pole due to the current-mode sampling effect, which can be approximately placed at 1/2 the per-phase switching frequency.

As a rule-of-thumb, the loop should be designed to close between 1/5th and 1/10th of the per-phase switching frequency. At this point, a determination should be made as to which of the following cases applies to the desired crossover frequency:

- **Case 1:** $\omega_{POLE} < 2\pi \times f_{CROSSOVER} < \omega_{ZERO}$

This case is likely to exist in situations where the zero frequency (ω_{ZERO}) is relatively high due to use of low-value output capacitors with low ESR (e.g., 560µF/7mΩ or all-ceramic designs).

Analysis of the control-to-output transfer function for this case shows that 1) the slope is -1 at the crossover frequency due to the low-frequency pole (ω_{POLE}), and 2) the compensation must provide gain boost at the crossover frequency to bring the loop gain to zero at crossover. Because of item 1), the compensator gain must be flat at crossover so that the closed-loop gain rolls off with -1 slope at crossover.

For this case, it is recommended to design the compensator with type II compensation. The zero is placed to ensure flat gain at crossover, and the 2nd pole provides phase shift above crossover. The compensator consists of a series resistor (R_{COMP}) and capacitor (C_{COMP1}) from COMP to GND, and a second capacitor (C_{COMP2}) placed from COMP to GND, in parallel to R_{COMP} and C_{COMP1} (see Figure 11).

The first step in the compensator design is to choose the desired phase margin at crossover and solve for the error-amplifier phase shift:

$$\phi_{ERROR\_AMPLIFIER} = \phi_{MARGIN} - \phi_{CONTR\_OUTPUT}$$

where ϕ_{MARGIN} is the desired phase margin at crossover, and ϕ_{CONTR_OUTPUT} is the phase shift from control-to-output (at crossover).

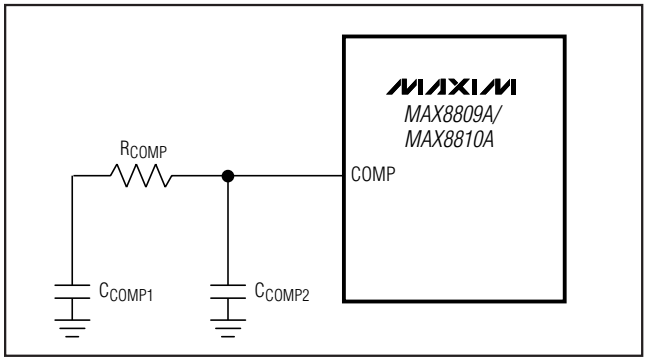

Figure 11. Type II Compensation Scheme

The next step is to determine the constant K value in the equation below, which provides the desired error-amplifier phase shift determined above. The value of K determines the locations of the error-amplifier zero and high-frequency pole relative to the crossover frequency:

$$\phi_{ERROR\_AMPLIFIER} = \left(\arctan(K) - \arctan\left(\frac{1}{K}\right)\right) \times \frac{180}{\pi} + 90$$

$$\omega_{ZERO\_ERROR\_AMPLIFIER} = \frac{2\pi \times f_{CROSSOVER}}{K}$$

$$\omega_{POLE\_ERROR\_AMPLIFIER} = 2\pi \times f_{CROSSOVER} \times K$$

The simplified compensator transfer function can be modeled at low frequencies as:

$$g_{MV} \times \left(R_{COMP} + \frac{1}{\omega \times C_{COMP1}}\right)$$

where g_{MV} is the transconductance of the error amplifier. At crossover, C_{COMP1} is essentially a short and can be ignored. The compensator must provide gain boost to bring the loop gain to zero at crossover. Applying these criteria and solving for R_{COMP}:

$$R_{COMP} = \frac{1}{g_{MV} \times |G_{CONTR\_OUTPUT}(f_{CROSSOVER})|}$$

Solving for C_{COMP1} and C_{COMP2} is now relatively straightforward:

$$C_{COMP1} = \frac{1}{\omega_{ZERO\_ERROR\_AMPLIFIER} \times R_{COMP}}$$

$$C_{COMP2} = \frac{1}{\omega_{POLE\_ERROR\_AMPLIFIER} \times R_{COMP}}$$

- **Case 2:** $\omega_{ZERO} < 2\pi \times f_{CROSSOVER} < \omega_{POLE\text{-}CM}$

where $\omega_{POLE\text{-}CM}$ is the frequency of the double pole created by the sampling effect. This case is likely to exist in situations where high-capacitance, high-ESR output capacitors (e.g., low-cost aluminum electrolytic such as 2800µF/12mΩ) are used.

Analysis of the control-to-output transfer function for this case shows that 1) the slope is zero at crossover so the compensation must roll off with a -1 slope, and 2) the compensation must provide gain boost at the crossover frequency to bring the loop gain to zero at crossover. Both of these conditions are satisfied with the following relationship:

$$g_{MV} \times \frac{1}{2\pi \times f_{CROSSOVER} \times C_{COMP}} = \frac{1}{|G_{CONTR\_OUTPUT}(f_{CROSSOVER})|}$$

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where g_{MV} is the transconductance of the error amplifier and C_{COMP} is a capacitor placed from the output of the error amplifier (COMP) to GND. Solving for C_{COMP}:

$$C_{COMP} = g_{MV} \times \frac{|G_{CONTR\_OUTPUT}(f_{CROSSOVER})|}{2\pi \times f_{CROSSOVER}}$$

Multiload-Line Programming (MAX8810A)

In some applications, it may be desired to implement multiple load-lines. This is easily accomplished by switching resistors in parallel with R_{LL} (Figure 12). Paralleling resistors with R_{LL} causes the load-line resistance to increase. With this scheme implemented for the MAX8810A, the offset voltage is not affected by the new load-line setting. It is also not necessary to change the temperature compensation based on the new load-line setting. Switches S1 and S2 can be implemented with small-signal n-channel MOSFETs.

R_{LL1} and R_{OS} are designed using methods described in the *Loop-Compensation Design* section. R_{O1}, R_{O2}, and R_{O3} are the required load-line resistances. R_{LL2} and R_{LL3} are calculated as follows:

$$R_{COMP1} = R_{LL} \parallel R_{OS}$$

$$R_{LL2} = \frac{R_{COMP1} \times R_{COMP2}}{R_{COMP1} - R_{COMP2}}$$

where:

$$R_{COMP2} = \frac{R_{O1}}{R_{O2}} \times R_{COMP1}$$

and:

$$R_{COMP1} = \frac{R_{LL1} \times R_{OS}}{R_{LL1} + R_{OS}}$$

$$R_{LL3} = \frac{R_{COMP2} \times R_{COMP3}}{R_{COMP2} - R_{COMP3}}$$

where:

$$R_{COMP3} = \frac{R_{O2}}{R_{O3}} \times R_{COMP2}$$

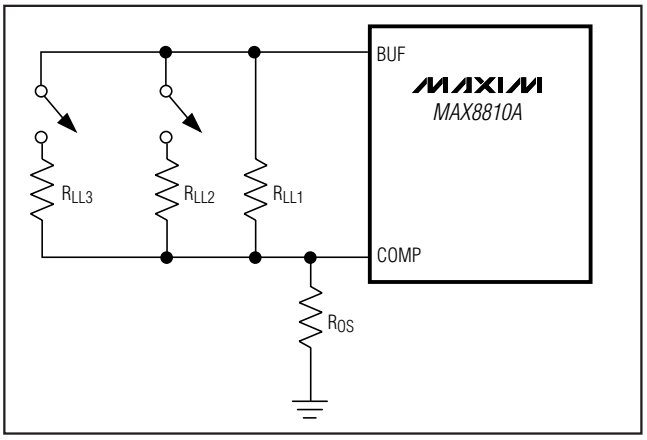

Figure 12. Load-Line Switching Circuit

Setting the Current Limit

The current-limit threshold sets the maximum available output DC current. The output current limit should be selected to meet the OTF requirement as described in the *Output Capacitor Selection* section. The voltage at ILIM and the value of the current-sense resistor or the DC resistance of the output inductor sets the current-limit threshold:

$$V_{ILIM} = G_{CA} \times R_{SENSE} \times \frac{I_{LIM}}{N}$$

where R_{SENSE} is the resistance of the current-sensing element. The value of R_{SENSE} at room temperature must be used because the MAX8809A and MAX8810A provide temperature-compensated current limit. V_{ILIM} is set by connecting ILIM to the center tap of a resistor-divider from REF to GND. Select R1 and R3 (Figure 13) so the current through the divider is at least 10µA:

$$R1 + R3 < 200k\Omega$$

A typical value for R1 is 10kΩ; then solve for R3 using:

$$R3 = R1 \times \frac{V_{LIM}}{2 - V_{LIM}}$$

Applications Information

PC Board Layout Guidelines

A properly designed PC board layout is important in any switching DC-DC converter circuit. Mount the MOSFETs, inductors, input/output capacitors, and current-sense resistor on the top side of the PC board. A single large ground plane is preferred; however it is very important to partition the 'analog' portion of this ground plane from the 'power' portion of the ground plane. Ensure that all analog ground connections are made to the ground plane away from any areas of power ground switching currents. Do not connect the analog returns at a single point to the ground plane; use as many direct connections as possible. Connect the GND of the IC to the thermal pad of the IC on the top layer. Connect the thermal pad to the ground plane through at least nine 10-mil drill size VIAs.

To help dissipate heat, place high-power components (MOSFETs and inductors) on a large copper area, or use a heat sink. Keep high-current traces short, wide, and tightly coupled to reduce trace inductances and resistances. Gate-drive traces should be at least 20 mils wide, kept as short as possible, and tightly coupled to reduce EMI and ringing induced by high-frequency gate currents. Adjacent DH_ and LX_ traces should be tightly coupled. Connect the PGND_ pins to the ground plane near the controller through two VIAs (each).

A clean current-sense signal is critical to a successful layout. Always place the current-sense traces on the bottom layer. Make sure all adjacent traces (for example CS1+, CS2+, and CS12-) are tightly coupled. Kelvin connections to the current-sense element are essential. For inductor DCR current-sensing, place all current-sense components near the inductor, except for the filtering capacitors, which should be placed next to the controller IC. This ensures that noise generated by large di/dt on the LX node is kept away from both current-sense signals and the controller IC. To ensure the integrity of the current-sense signal, the inner layer above the bottom layer must be a solid ground plane.

Place the VL_ decoupling capacitor on the top layer and near the VL_ pins. The negative terminal of the VL_ decoupling capacitor should be connected to PGND_ on the top layer. Also place the BST capacitors on the top layer near the controller. When needed always use double VIAs on the driver traces to reduce inductance. Do not connect the PGND_ pins to the thermal pad on the top layer.

The NTC thermistor should be placed near the "hottest" inductor. Use two traces, tightly coupled, to return to the controller. To ensure temperature compensation accuracy, make sure that the GND trace of the NTC is not "accidentally" connected to any other GND trace or ground plane on the way back to the controller.

Place the BUF capacitor, REF capacitor, VCC capacitor, the current-sense decoupling capacitors, and the remote-sense decoupling capacitors as close to the MAX8809A/MAX8810A as possible. All decoupling capacitors must make a direct connection to the corresponding pin. Making the connection using VIAs to transition between layers creates parasitic inductance, which negates the benefit of the decoupling capacitor. If this cannot be avoided, use double VIAs to minimize the parasitic inductance.

A sample layout is available in the evaluation kit to speed designs.

Chip Information

PROCESS: BiCMOS

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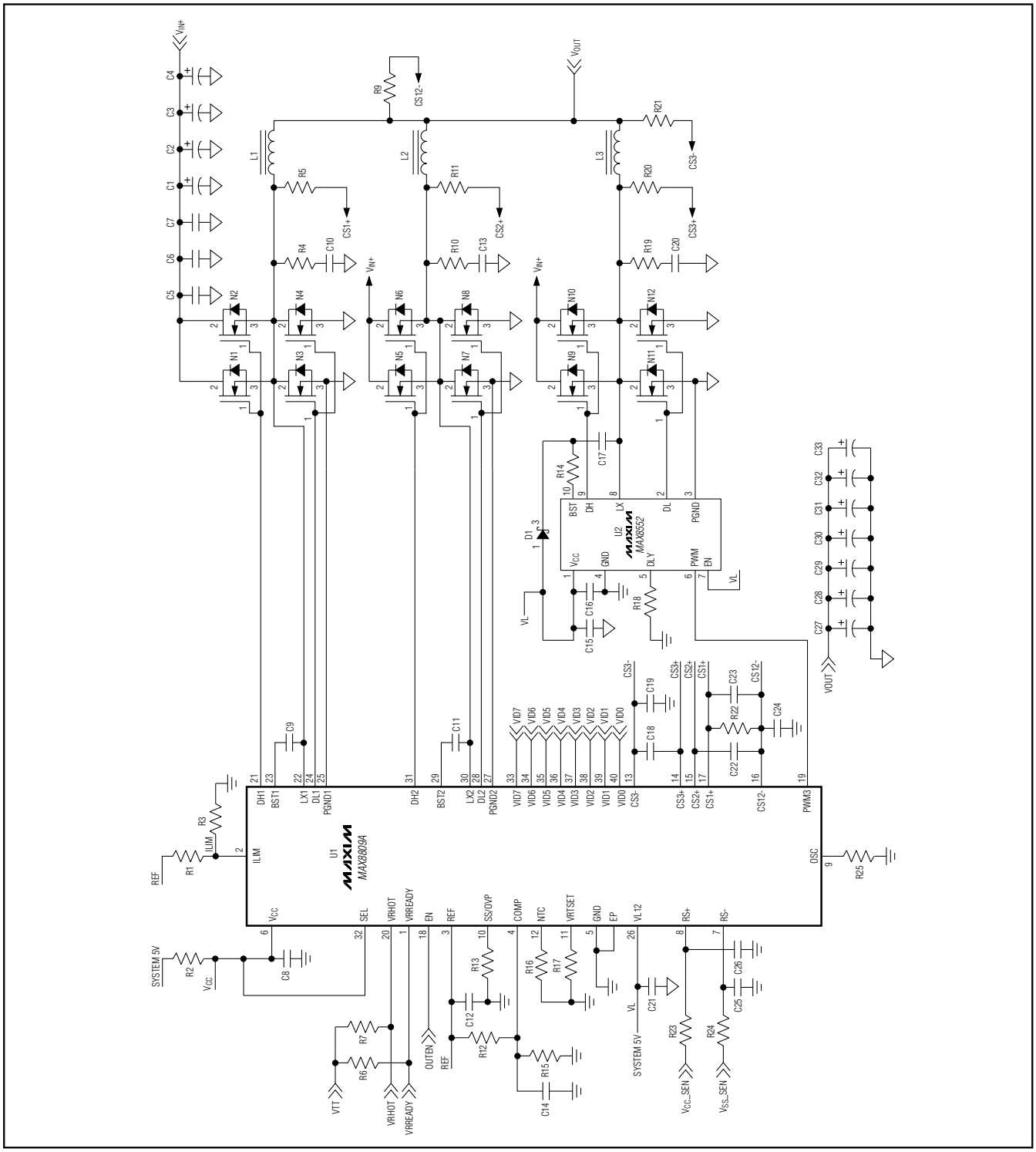


Figure 13. Intel VRD11 Desktop Application Circuit Using the MAX8809A—3-Phase, 85A

Table 8. Bill of Materials for Intel VRD11 3-Phase Desktop Application Circuit (Figure 13)

COMPONENTS	DESCRIPTION	PART NUMBER
C1–C4	1500µF, 16V aluminum electrolytic capacitors	Rubycom 16VMBZ1500
C5, C6, C7	10µF, 16V X5R ceramic capacitors (1206)	Taiyo Yuden EMK316BJ106ML
C8, C15, C21	2.2µF, 10V X5R ceramic capacitors (0603)	Taiyo Yuden LMK107BJ225MA
C9, C11, C12, C16, C17	0.22µF, 16V X5R ceramic capacitors (0603)	Taiyo Yuden EMK107BJ224KA
C10, C13, C20	2200pF, 50V X7R ceramic capacitors (0603)	TDK C1608X7R1H222K
C14	68pF, 50V C0G ceramic capacitor (0603)	Kemet C0603C101J5GACTU
C18, C22, C23	0.22µF, 10V X5R ceramic capacitors (0603)	TDK C1608X5R1A224K
C19, C24, C25, C26	1000pF, 50V X7R ceramic capacitors (0603)	Kemet C0603C102J5RACTU
C27–C33	560µF, 4V, 7mΩ ESR OS-CON capacitors	Sanyo 4R5SEP560M
D1	30V, 200mA Schottky diode (SOT23)	Central Semiconductor CMPSH-3
L1, L2, L3	0.20µH, 30A toroid cores	Falco T50069
N1, N2, N5, N6, N9, N10	30V, 12mΩ n-channel logic MOSFETs (DPAK)	International Rectifier IRLR7821
N3, N4, N7, N8, N11, N12	30V, 4.5mΩ n-channel logic MOSFETs (DPAK)	International Rectifier IRLR7843
R1	10kΩ ±1% resistor (0603)	—
R2	10Ω ±5% resistor (0603)	—
R15	5.62kΩ ±1% resistor (0603)	—
R4, R9, R10, R19, R21	2.2Ω ±5% resistors (0603)	—
R5, R11, R20	1.62kΩ ±1% resistors (0603)	—
R6, R7	680Ω ±1% resistors (0603)	—
R3, R12	8.06kΩ ±1% resistors (0603)	—
R13	22kΩ ±5% resistor (0603)	—
R14	0Ω ±5% resistor (0603)	—
R16	10kΩ NTC thermistor	Panasonic ERTJ1VR103
R17	61.9kΩ ±1% resistor (0603)	—
R18	7.1kΩ ±1% resistor (0603)	—
R22	Not installed	
R23, R24	100Ω ±1% resistors (0603)	—
R25	220kΩ ±1% resistor (0603)	—
U1	VRD11, VRD10, and K8 Rev F 3-phase controller	Maxim MAX8809A
U2	High-speed, single-phase MOSFET driver	Maxim MAX8552

VRD11/VRD10, K8 Rev F 2/3/4-Phase PWM Controllers with Integrated Dual MOSFET Drivers

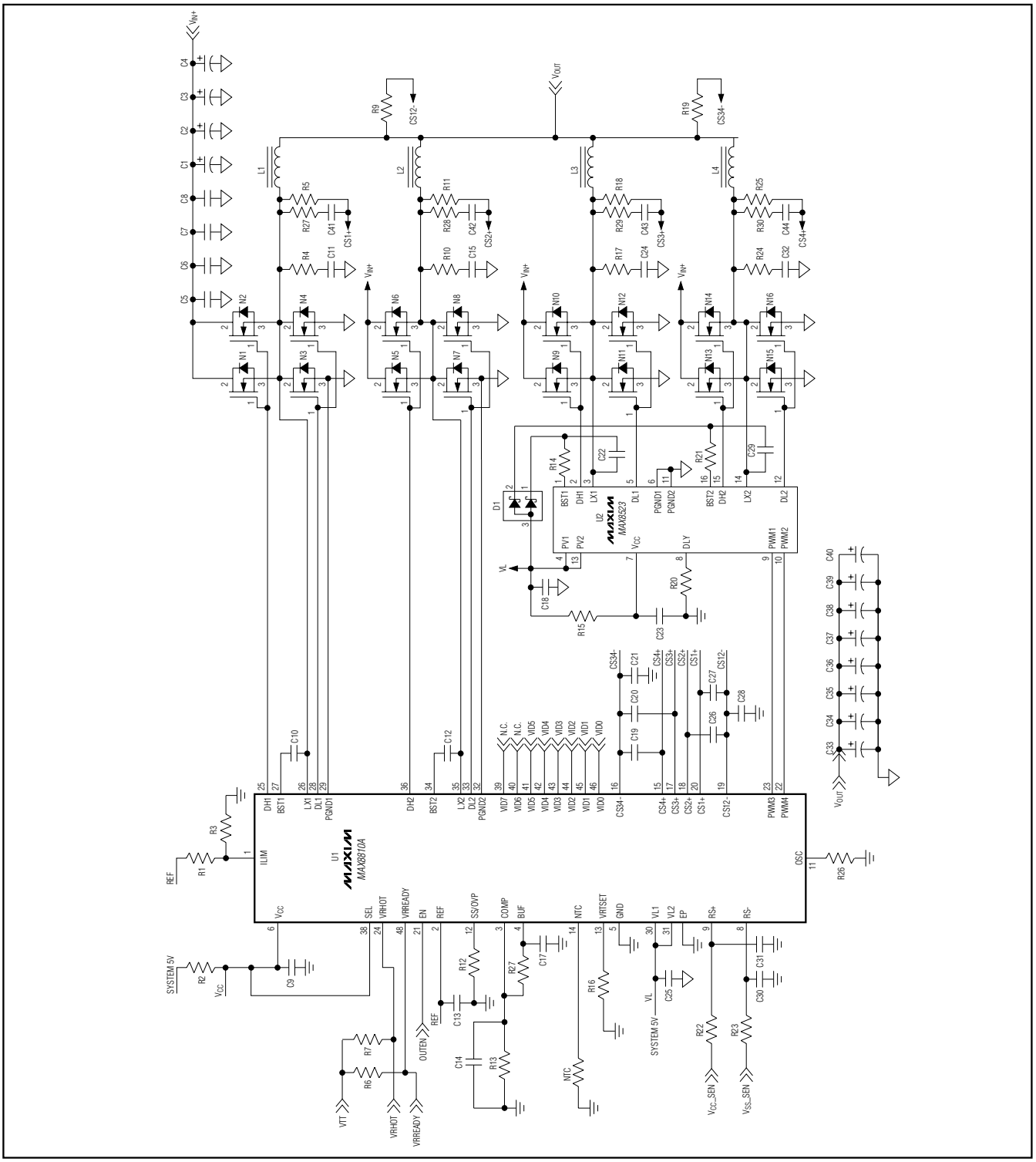


Figure 14. Intel VRD11 Desktop Application Circuit Using the MAX8810A—4-Phase, 115A

Table 9. Bill of Materials for Intel VRD11 4-Phase Desktop Application Circuit (Figure 14)

COMPONENTS	DESCRIPTION	PART NUMBER
C1–C4	1500µF, 16V aluminum electrolytic capacitors	Rubycom 16VMBZ1500
C5–C8	10µF, 16V X5R ceramic capacitors (1206)	Taiyo Yuden EMK316BJ106ML
C9, C17, C18, C25	2.2µF, 10V X5R ceramic capacitors (0603)	Taiyo Yuden LMK107BJ225MA
C10, C12, C13, C22, C29	0.22µF, 16V X5R ceramic capacitors (0603)	Taiyo Yuden EMK107BJ224KA
C11, C15, C24, C32	2200pF, 50V X7R ceramic capacitors (0603)	TDK C1608X7R1H222K
C14	68pF, 50V C0G ceramic capacitor (0603)	Kemet C0603C101J5GACTU
C19, C20, C26, C27	0.22µF, 10V X5R ceramic capacitors (0603)	TDK C1608X5R1A224K
C21, C28, C30, C31	1000pF, 50V X7R ceramic capacitors (0603)	Murata C0603C102J5RACTU
C33–C40	560µF, 4V, 7mΩ ESR OS-CON capacitors	Sanyo 4R5SEP560M
D1	30V, 200mA Schottky diode (SOT23)	Central Semiconductor CMPSH-3A
L1–L4	0.20µH, 30A toroid cores	Falco T50069
N1, N2, N5, N6, N9, N10, N13, N14	30V, 12mΩ n-channel logic MOSFETs (DPAK)	International Rectifier IRLR7821
N3, N4, N7, N8, N11, N12, N15, N16	30V, 4.5mΩ n-channel logic MOSFETs (DPAK)	International Rectifier IRLR7843
R1	10kΩ ±1% resistor (0603)	—
R2, R15	10Ω ±5% resistors (0603)	—
R3	7.15Ω ±1% resistor (0603)	—
R4, R9, R10, R17, R19, R24	2.2Ω ±5% resistors (0603)	—
R5, R11, R18, R25	1.62kΩ ±1% resistors (0603)	—
R6, R7	680Ω ±1% resistors (0603)	—
R12	22.0kΩ ±1% resistor (0603)	—
R13	26.1kΩ ±1% resistor (0603)	—
R14, R21	0Ω ±5% resistors (0603)	—
R16	61.9kΩ, ±1% resistor (0603)	—
R20	7.17Ω ±1% resistor (0603)	—
R22, R23	100Ω ±1% resistors (0603)	—
R26	160kΩ ±1% resistor (0603)	—
R27	2.87kΩ ±1% resistor (0603)	—
NTC	10kΩ NTC thermistor	Panasonic ERTJ1VR103
U1	VRD11, VRD10, and K8 Rev F 4-phase controller	Maxim MAX8810A
U2	High-speed, dual-phase MOSFET driver	Maxim MAX8523

VRD11/VRD10, K8 Rev F 2/3/4-Phase PWM Controllers with Integrated Dual MOSFET Drivers

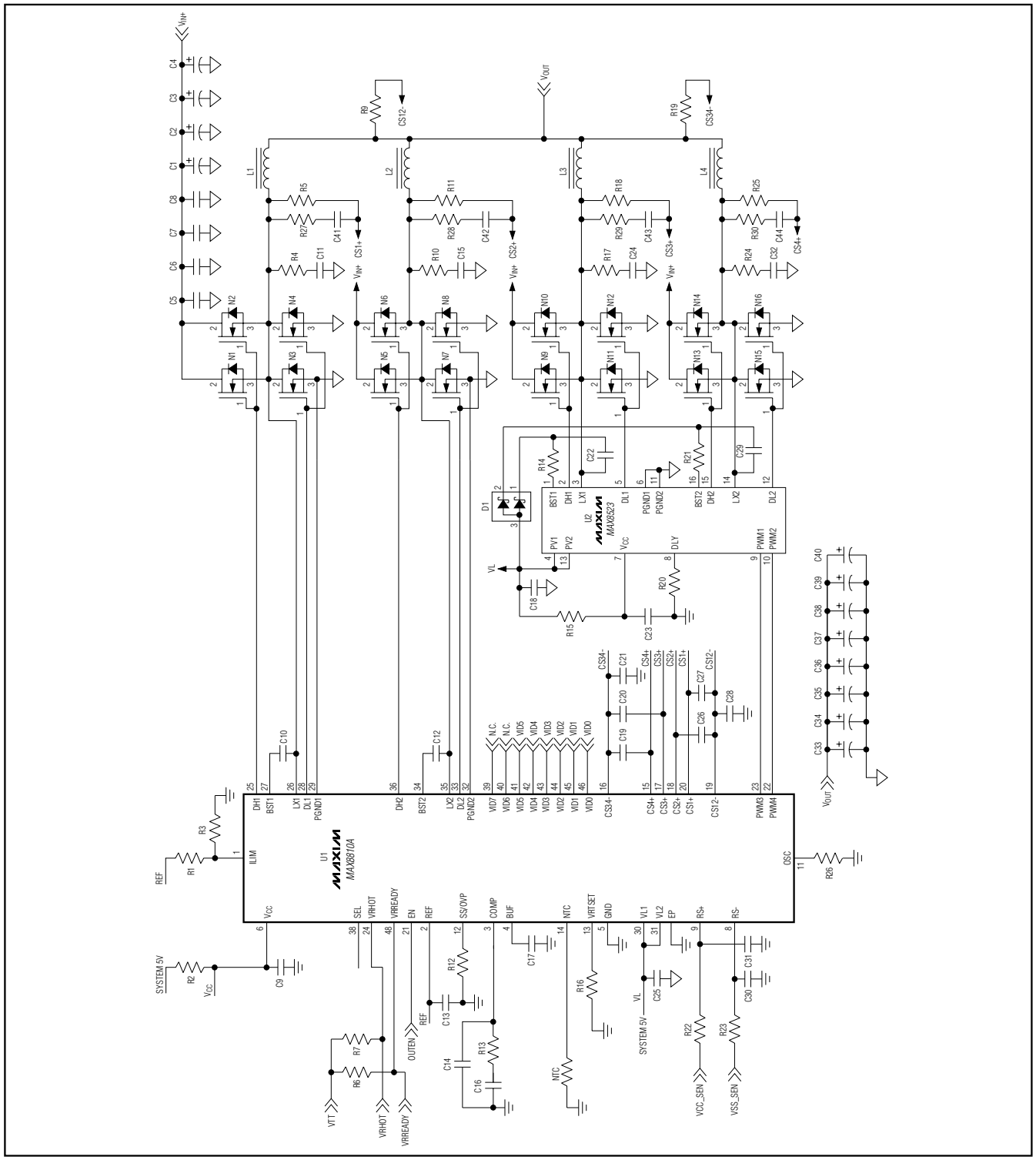


Figure 15. AMD K8 Rev F Desktop Application Circuit Using the MAX8810A—4-Phase, 115A

Table 10. Bill of Materials for AMD K8 Rev F Desktop Application Circuit (Figure 15)

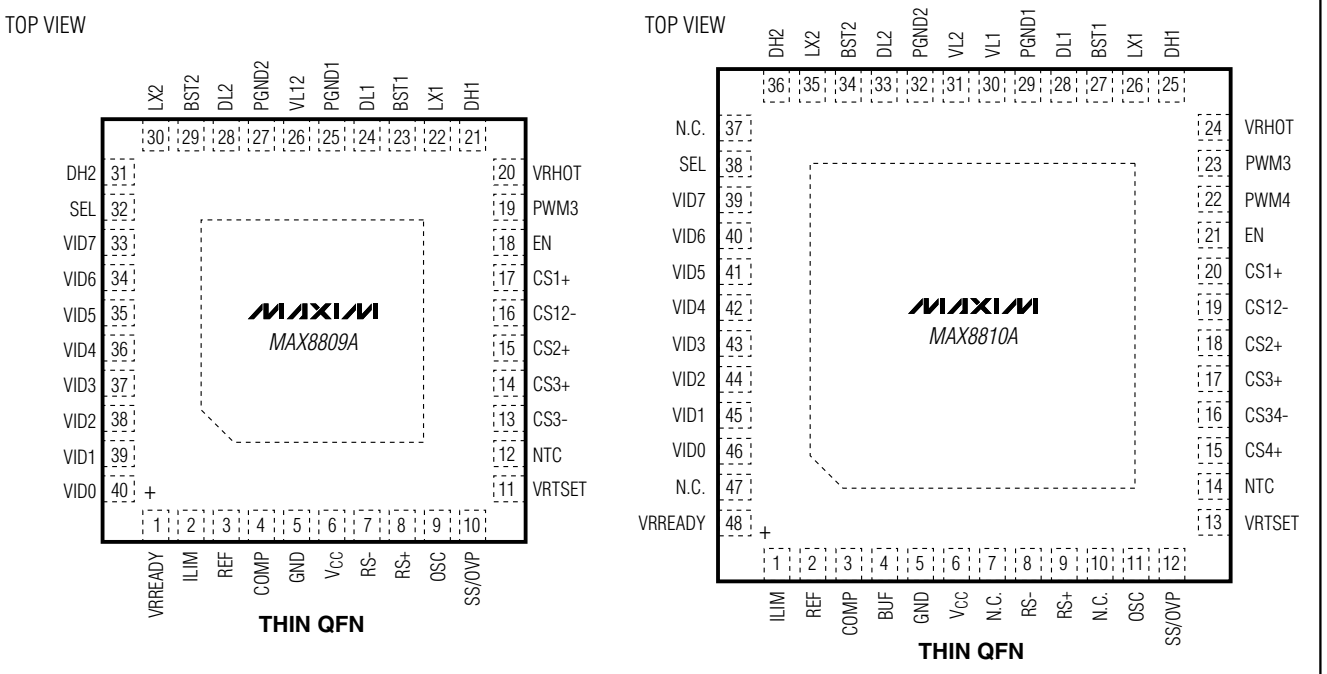
COMPONENTS	DESCRIPTION	PART NUMBER
C1–C4	1500µF, 16V aluminum electrolytic capacitors	Rubycom 16VMBZ1500
C5–C8	10µF, 16V X5R ceramic capacitors (1206)	Taiyo Yuden EMK316BJ106ML
C9, C17, C18, C25	2.2µF, 10V X5R ceramic capacitors (0603)	Taiyo Yuden LMK225BJ225ML
C10, C12, C13, C22, C29	0.22µF, 10V X5R ceramic capacitors (0603)	Taiyo Yuden EMK107BJ224KA
C11, C15, C24, C32	2200pF, 50V X7R ceramic capacitors (0603)	TDK C1608X7R1H222K
C14	Not installed (0603)	—
C16	0.015µF, 50V C0G ceramic capacitor (0603)	Murata GRM39X7R153K50
C19, C20, C23, C26, C27	0.22µF, 10V X5R ceramic capacitors (0603)	TDK C1608X5R1A224K
C21, C28, C30, C31	1000pF, 50V X7R ceramic capacitors (0603)	Kemet C0603C102J5RACTU
C33–C40	2200µF, 6.3V, 12mΩ ESR aluminum electrolytic capacitors	Rubycon 6.3VMBZ2200
C41–C44	Not installed (0603)	—
D1	30V, 200mA Schottky diode (SOT23)	Central Semiconductor CMPSH-3A
L1–L4	0.28µH, 30A toroid cores	Falco T50183
N1, N2, N5, N6, N9, N10, N13, N14	30V, 12mΩ n-channel logic MOSFETs (DPAK)	International Rectifier IRLR7821
N3, N4, N7, N8, N11, N12, N15, N16	30V, 4.5mΩ n-channel logic MOSFETs (DPAK)	International Rectifier IRLR7843
R1	10kΩ ±1% resistor (0603)	—
R2, R15	10Ω ±5% resistors (0603)	—
R3 R4, R9, R10, R17, R19, R24	7.15kΩ ±1% resistor (0603) 2.2Ω ±5% resistors (0603)	— —
R5, R11, R18, R25	1.62kΩ ±1% resistors (0603)	—
R6, R7	680Ω ±1% resistors (0603)	—
R12	22.0kΩ ±1% resistor (0603)	—
R13	4.32kΩ ±1% resistor (0603)	—
R14, R21	0Ω ±5% resistors (0603)	—
R16	61.9kΩ ±1% resistor (0603)	—
R20	7.10kΩ ±1% resistor (0603)	—
R22, R23	100Ω ±11% resistors (0603)	—
R26	160kΩ ±1% resistor (0603)	—
R27–R30	Not installed (0603)	—
NTC	10kΩ NTC thermistor	Panasonic ERTJ1VR103
U1	VRD11, VRD10, and K8 Rev F 4-phase	Maxim MAX8810A
U2	High-speed, dual-phase MOSFET driver	Maxim MAX8523

VRD11/VRD10, K8 Rev F 2/3/4-Phase PWM Controllers with Integrated Dual MOSFET Drivers

Table 11. Suggested Component Suppliers

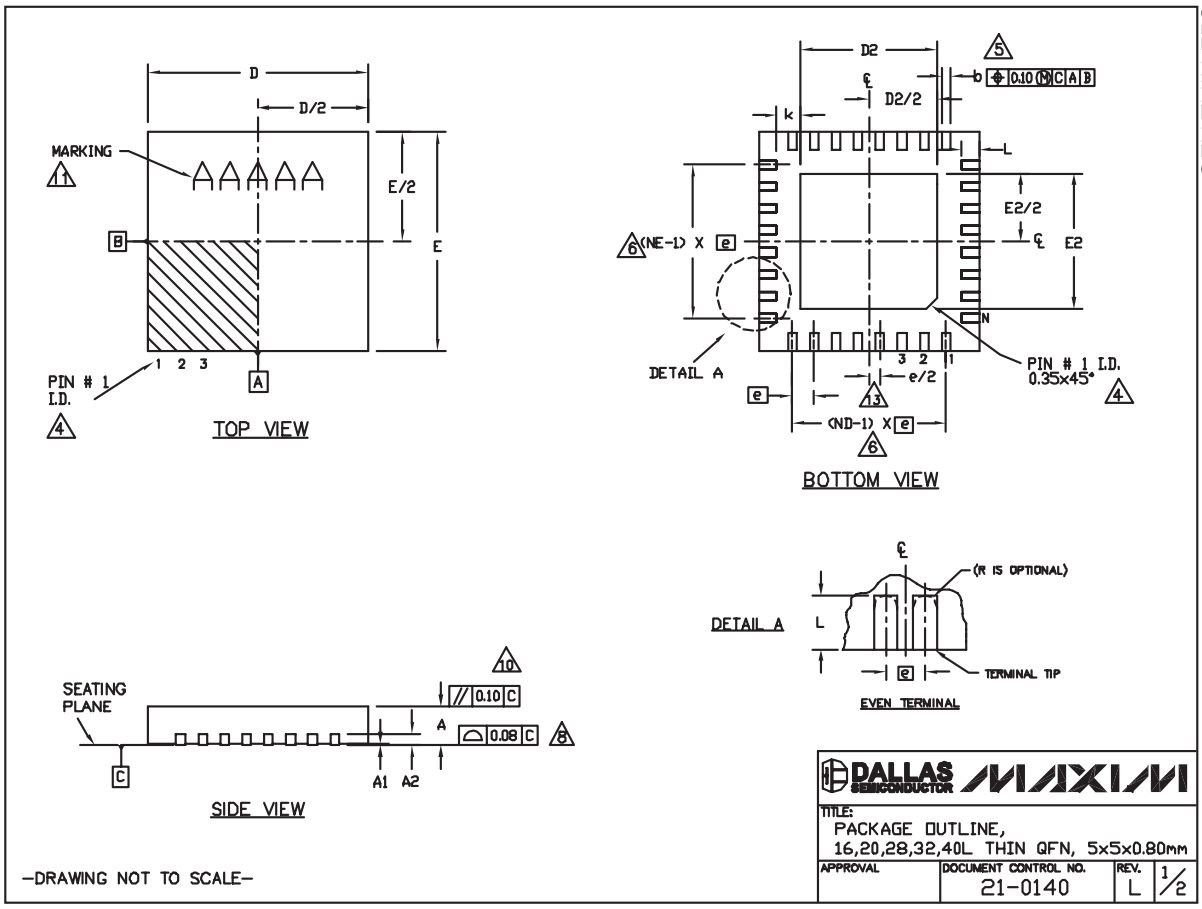
COMPONENT SUPPLIER	PHONE	FAX	WEBSITE
BI Technologies	714-447-2300	714-388-0046	www.bitechnologies.com
Falco	305-662-7276	928-752-3256	www.falco.com
International Rectifier	310-252-7105	310-252-7903	www.irf.com
Kemet	864-963-6300	408-986-1442	www.kemet.com
Murata	770-436-1300	770-436-3030	www.murata.com
Pulse	215-781-6400	215-781-6403	www.pulseeng.com
Panasonic	800-344-2112	—	www.panasonic.com
Sanyo	619-661-6835	619-661-1055	www.sanyo.com
Taiyo Yuden	81-3-3833-5441	81-3-3835-4754	www.t-yuden.com
TDK	408-437-9585	408-437-9591	www.component.tdk.com

Pin Configurations



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



VRD11/VRD10, K8 Rev F 2/3/4-Phase PWM Controllers with Integrated Dual MOSFET Drivers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED AND PbFREE PARTS.

–DRAWING NOT TO SCALE–

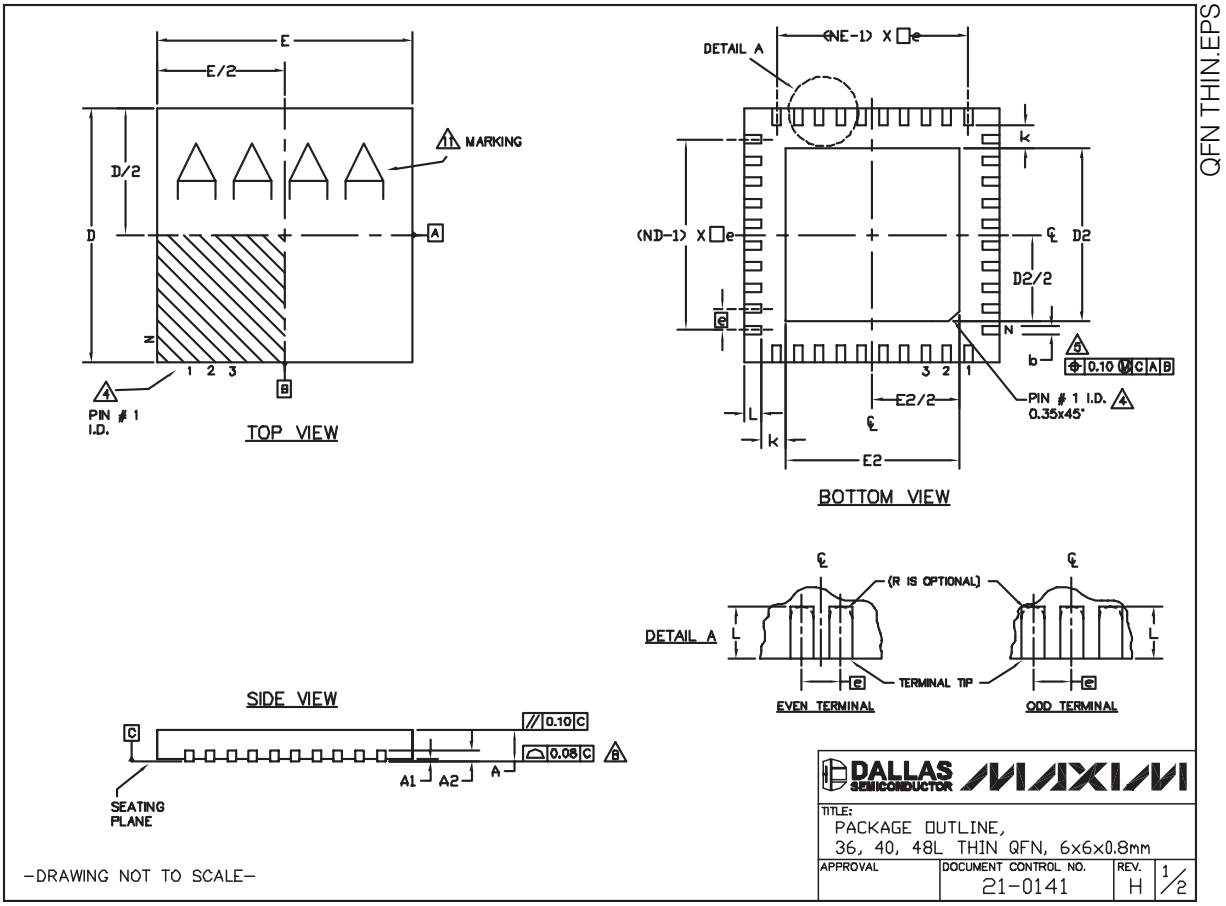
DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.80mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	L	2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



VRD11/VRD10, K8 Rev F 2/3/4-Phase PWM Controllers with Integrated Dual MOSFET Drivers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80
T3666N-1	3.60	3.70	3.80	3.60	3.70	3.80
T3666MN-1	3.60	3.70	3.80	3.60	3.70	3.80
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20
T4866-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866-2	4.40	4.50	4.60	4.40	4.50	4.60

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN FOR REFERENCE ONLY.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 36, 40, 48L THIN QFN, 6x6x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0141	H	2/2

Revision History

Pages changed at Rev 1: 1–6, 8, 13–16, 19, 20, 22, 30-37, 40, 43.