Panasonic

NN30500A

http://www.semicon.panasonic.co.jp/en/

2-Channel 6A Synchronous DC-DC Step down Regulator with LDO Regulator

FEATURES

- 2-Channel high-speed response DC-DC Step Down Regulator circuit that employs Hysteretic Control System
- Hi-side 20 mΩ (Typ.) and Low-side 20 mΩ (Typ.) MOSFETs for High Efficiency at 6 A
- Skip (discontinuous) Mode for Light Load Efficiency
- Maximum Output Current : 6 A
- Input Voltage Range : PV_{IN1}=PV_{IN2} = 4.5 V to 24 V
- Output Voltage Range : 0.75 V to 5.5 V
- Optimized frequency for efficiency : 600 kHz
- Internal Soft Start for component reduction
- 2.5V (100mA) LDO built-in (PHY)
- Two external MOS control switch (CNT)
- Low Operating and Standby Quiescent Current
- PowerGood Indication for Output Over/Under voltage
- Built-in :
  Under Voltage Lockout (UVLO),
  Thermal Shut Down (TSD),
  Over/Under Voltage Detection (OVD/UVD),
  Over Current Protection (OCP),
  Short Circuit Protection (SCP)
- 32 pin Plastic Quad Flat Non-leaded Package Heat Slug Down (QFN Type)
  (Size : 4 mm X 5 mm X 0.8 mm, 0.5 mm pitch)

DESCRIPTION

NN30500A is a 2-Channel synchronous DC-DC Step down Regulator comprising of a Controller IC and four power MOSFETs and employs the hysteretic control system.

By this system, when load current changes suddenly, it responds at high speed and minimizes the changes of output voltage.

It is possible to use capacitors with small capacitance and it is unnecessary to add external parts for system phase compensation, this IC realizes downsizing of set and reducing in the number of external parts.

Output voltage is adjustable by user.

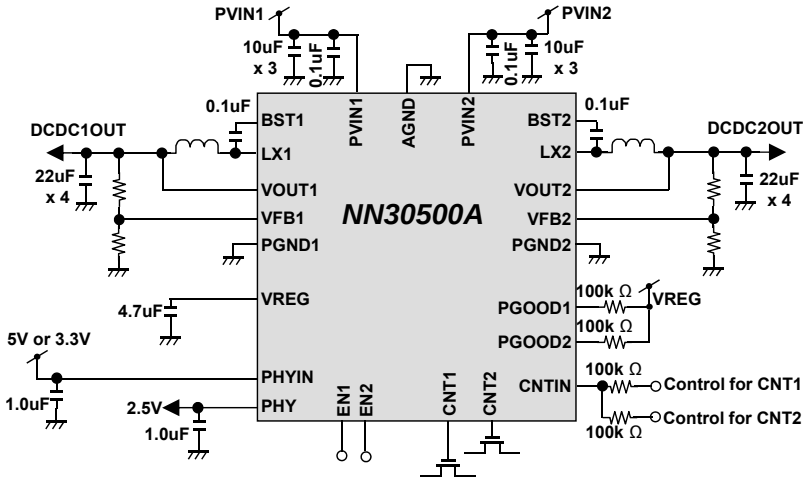
Maximum current for DCDC1 and DCDC2 are 6 A.

APPLICATIONS

High Current Distributed Power Systems such as

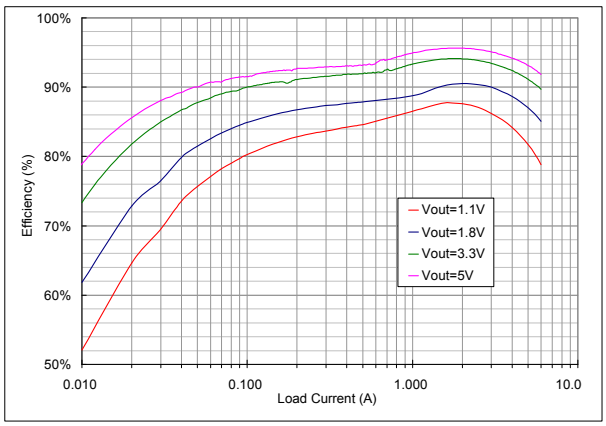
- SSDs (Solid State Drives)
- PCs
- Servers
- Security Cameras
- Network TVs
- OA Equipment, etc.

TYPICAL APPLICATION



Note:
The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

EFFICIENCY CURVE



Condition:
V_{IN} = 12 V
C_{OUT} = 88 µF (22 µF x 4)
Frequency = 600 kHz
L_{OUT} = 1.0 µH (V_{OUT} = 1.1 V & 1.8 V)
L_{OUT} = 2.2 µH (V_{OUT} = 3.3 V)
L_{OUT} = 3.3 µH (V_{OUT} = 5 V)

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Panasonic NN30500A

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ORDERING INFORMATION

Order Number	Feature	Package	Packing Form
NN30500A-VB	Maximum Output Current : 6A	32 pin HQFN	Emboss taping

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage	V_{IN}	30	V	*1
	V_{PHYIN}	6.0	V	*1
Operating free-air temperature	T_{opr}	– 40 to + 85	°C	*2
Operating junction temperature	T_j	– 40 to + 150	°C	*2
Storage temperature	T_{stg}	– 55 to + 150	°C	*2
Input Voltage Range	V_{OUT1}, V_{FB1}, V_{OUT2}, V_{FB2}	– 0.3 to (V_{REG} + 0.3)	V	*1 *3
	V_{EN1}, V_{EN2}, V_{CNTIN}	– 0.3 to 6.0	V	*1
Output Voltage Range	V_{PGOOD1}, V_{PGOOD2}, V_{CNT1}, V_{CNT2}	– 0.3 to (V_{REG} + 0.3)	V	*1 *3
	V_{LX1}, V_{LX2}	– 0.3 to (V_{IN} + 0.3)	V	*1 *4
ESD	HBM	2	kV	—

Note: Do not apply external currents and voltages to any pin not specifically mentioned.

This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected. V_{IN} is voltage for PVIN1 and PVIN2. $V_{IN} = PV_{IN1} = PV_{IN2}$.

*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25 °C.

*3 : (V_{REG} + 0.3) V must not exceed 6 V.

*4 : (V_{IN} + 0.3) V must not exceed 30 V.

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POWER DISSIPATION RATING

Package	θ_{j-a}	θ_{j-c}	P_D (Ta = 25 °C)	P_D (Ta = 85 °C)	Note
32 pin Plastic Quad Flat Non-leaded Package Heat Slug Down (QFN Type)	48.8 °C /W	6.1 °C /W	2.561 W	1.332 W	*1
	33.4 °C /W	4.3 °C /W	3.743 W	1.946 W	*2

Note: For the actual usage, please refer to the P_D-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.
*1:Glass Epoxy Substrate (4 Layers) [50 X 50 X 0.8 t (mm)]
*2:Glass Epoxy Substrate (4 Layers) [50 X 50 X 1.57 t (mm)] + Thermal vias

CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Min	Typ	Max	Unit	Note
Supply voltage range	PV_{IN1}	4.5	12	24	V	—
	PV_{IN2}	4.5	12	24	V	—
	V_{PHYIN}	3.0	5.0	5.5	V	—
Input Voltage Range	V_{EN1}	– 0.3	—	5.0	V	—
	V_{EN2}	– 0.3	—	5.0	V	—
	V_{CNTIN}	– 0.3	—	5.0	V	—
Output Voltage Range	V_{PGOOD1}	– 0.3	—	V_{REG} + 0.3	V	*1
	V_{PGOOD2}	– 0.3	—	V_{REG} + 0.3	V	*1
	V_{CNT1}	– 0.3	—	V_{REG} + 0.3	V	*1
	V_{CNT2}	– 0.3	—	V_{REG} + 0.3	V	*1
	V_{LX1}	– 0.3	—	V_{IN} + 0.3	V	*2
	V_{LX2}	– 0.3	—	V_{IN} + 0.3	V	*2

Note: Voltage values, unless otherwise specified, are with respect to GND.
GND is voltage for AGND, PGND1 and PGND2. AGND = PGND1 = PGND2
V_{IN} is voltage for PVIN1 and PVIN2. $V_{IN} = PV_{IN1} = PV_{IN2}$.
Do not apply external currents or voltages to any pin not specifically mentioned.
*1 : (V_{REG} + 0.3) V must not exceed 6 V.
*2 : (V_{IN} + 0.3) V must not exceed 30 V.

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ELECTRICAL CHARACTERISTICS

DCDC1 & DCDC2 : C_{OUT} = 22 µF × 4, L_{OUT} = 1 µH, V_{OUT} Setting = 1.1 V, V_{IN} = 12 V,
Switching Frequency = 600 kHz, T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current Consumption							
Consumption current at active	I_{OPR}	V_{EN1} = V_{EN2} = 1.8 V I_{OUT1} = I_{OUT2} = 0 A R_{FB1} = 15kΩ, R_{FB2} =18kΩ DCDC No switching	—	1.20	2.40	mA	—
Consumption current at standby	I_{STB}	V_{EN1} = V_{EN2} = 0 V V_{PHYIN} = 5V	—	6	12	µA	—
	$I_{PHYINSTB}$		—	1	5	µA	—
Logic Pin Characteristics							
EN1 pin Low-level input voltage	V_{EN1L}	—	—	—	0.3	V	—
EN1 pin High-level input voltage	V_{EN1H}	—	1.5	—	5.0	V	—
EN1 pin leak current	$I_{leakEN1}$	V_{EN1} = 5 V	—	6.25	12.5	µA	—
EN2 pin Low-level input voltage	V_{EN2L}	—	—	—	0.3	V	—
EN2 pin High-level input voltage	V_{EN2H}	—	1.5	—	5.0	V	—
EN2 pin leak current	$I_{leakEN2}$	V_{EN2} = 5 V	—	6.25	12.5	µA	—
VREG Characteristics							
Output voltage	V_{REG}	I_{VREG} = 10 mA	5.30	5.50	5.70	V	—
Line regulation	$V_{REGLINE}$	V_{REGLIN} = V_{REG} (V_{IN}= 12 V) – V_{REG} (V_{IN} = 6 V) I_{VREG} = 10 mA	—	—	200	mV	—
Drop out voltage	V_{REGDO}	V_{IN} = 4.5 V I_{VREG} = 10 mA	4.11	—	—	V	—

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ELECTRICAL CHARACTERISTICS (Continued)

DCDC1 & DCDC2 : C_{OUT} = 22 µF × 4, L_{OUT} = 1 µH, V_{OUT} Setting = 1.1 V, V_{IN} = 12 V,
Switching Frequency = 600 kHz, T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
PHY LDO Characteristics							
PHYIN consumption current	I_{PHYIN}	I_{PHY} = 0 mA	—	43	86	uA	—
Output voltage 1	V_{PHY1}	V_{PHYIN} = 5V I_{PHY} = 10mA	2.375	2.500	2.625	V	—
Output voltage 1	V_{PHY2}	V_{PHYIN} = 5V I_{PHY} = 100mA	2.375	2.500	2.625	V	—
Line regulation	$V_{PHYLINE}$	$V_{PHYLINE}$ = V_{PHY} (V_{PHYIN}=5 V) – V_{PHY} (V_{PHYIN} = 3 V) I_{PHY} = 10 mA	—	—	50	mV	—
VFB Characteristics							
VFB1 comparator threshold	V_{FB1TH}	—	0.594	0.600	0.606	V	—
VFB1 pin leak current 1	$I_{leakF11}$	V_{FB1} = 0 V	– 1	—	1	µA	—
VFB1 pin leak current 2	$I_{leakF12}$	V_{FB1} = 5 V, V_{EN1} = V_{EN2} = 0 V	– 1	—	1	µA	—
VFB2 comparator threshold	V_{FB2TH}	—	0.594	0.600	0.606	V	—
VFB2 pin leak current 1	$I_{leakF21}$	V_{FB2} = 0 V	– 1	—	1	µA	—
VFB2 pin leak current 2	$I_{leakF22}$	V_{FB2} = 5 V, V_{EN1} = V_{EN2} = 0 V	– 1	—	1	µA	—
Under Voltage Lockout (UVLO)							
UVLO detection voltage	$V_{UVLODET}$	V_{IN} = 5 V to 0 V	3.6	3.8	4.0	V	—
UVLO recover voltage	$V_{UVLORST}$	V_{IN} = 0 V to 5 V	4.0	4.2	4.4	V	—

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ELECTRICAL CHARACTERISTICS (Continued)

DCDC1 & DCDC2 : C_{OUT} = 22 µF × 4, L_{OUT} = 1 µH, V_{OUT} Setting = 1.1 V, V_{IN} = 12 V,
Switching Frequency = 600 kHz, T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
PGOOD Characteristics							
PGOOD1 Threshold 1 (V_{FB} ratio for UVD detect)	V_{PG1UV}	V_{PGOOD1} : High to Low	77	85	93	%	—
PGOOD1 Hysteresis 1 (V_{FB} ratio for UVD release)	ΔV_{PG1UV}	V_{PGOOD1} : Low to High	3.5	5.0	6.5	%	—
PGOOD1 Threshold 2 (V_{FB} ratio for OVD detect)	V_{PG1OV}	V_{PGOOD1} : High to Low	107	115	123	%	—
PGOOD1 Hysteresis 2 (V_{FB} ratio for OVD release)	ΔV_{PG1OV}	V_{PGOOD1} : Low to High	3.5	5.0	6.5	%	—
PGOOD2 Threshold 1 (V_{FB} ratio for UVD detect)	V_{PG2UV}	V_{PGOOD2} : High to Low	77	85	93	%	—
PGOOD2 Hysteresis 1 (V_{FB} ratio for UVD release)	ΔV_{PG2UV}	V_{PGOOD2} : Low to High	3.5	5.0	6.5	%	—
PGOOD2 Threshold 2 (V_{FB} ratio for OVD detect)	V_{PG2OV}	V_{PGOOD2} : High to Low	107	115	123	%	—
PGOOD2 Hysteresis 2 (V_{FB} ratio for OVD release)	ΔV_{PG2OV}	V_{PGOOD2} : Low to High	3.5	5.0	6.5	%	—
CNT Characteristics							
CNTIN pin leak current	I_{CNTIN}	V_{CNTIN} = 5 V	—	—	2	uA	—
CNTIN threshold 1	V_{CNTIN1}	CNTIN = 0 V to 0.9 V	0.36	0.56	0.76	V	—
CNTIN threshold 2	V_{CNTIN2}	CNTIN = 0.9 V to 1.8 V	1.05	1.25	1.45	V	—
CNT1 charging current	I_{CNT1}	CNTIN = 1.8 V	-1.5	-1.0	-0.5	uA	—
CNT2 charging current	I_{CNT2}	CNTIN = 1.8 V	-1.5	-1.0	-0.5	uA	—

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ELECTRICAL CHARACTERISTICS (Continued)

DCDC1 & DCDC2 : C_{OUT} = 22 µF × 4, L_{OUT} = 1 µH, V_{OUT} Setting = 1.1 V, V_{IN} = 12 V,
Switching Frequency = 600 kHz, T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
DC-DC Characteristics							
DCDC1 Line regulation	$DD1_{LINE}$	PV_{IN1} = 6 V to 24 V I_{OUT1} = 0.5 A	—	0.25	0.75	%/V	—
DCDC1 Load regulation	$DD1_{LOAD}$	I_{OUT1} = 10 mA to 6 A	—	3.5	—	%	*1
DCDC1 Output ripple voltage 1	$DD1_{RPL1}$	I_{OUT1} = 10 mA	—	40	—	mV [p-p]	*1
DCDC1 Output ripple voltage 2	$DD1_{RPL2}$	I_{OUT1} = 3 A	—	20	—	mV [p-p]	*1
DCDC1 Load transient response 1	$DD1_{TR1}$	I_{OUT1} = 100 mA to 3 A Δt = 0.5 A / µs	—	20	—	mV	*1
DCDC1 Load transient response 2	$DD1_{TR2}$	I_{OUT1} = 3 A to 100 mA Δt = 0.5 A / µs	—	20	—	mV	*1
DCDC1 High Side Power MOSFET ON resistance	$DD1R_{ONH}$	V_{GS} = 5.0 V	—	20	40	mΩ	—
DCDC1 Low Side Power MOSFET ON resistance	$DD1R_{ONL}$	V_{GS} = 5.0 V	—	20	40	mΩ	—
DCDC1 MIN input and output voltage difference	$DD1V_{diff}$	$DD1V_{diff} = PV_{IN1} - V_{OUT1}$	—	1.5	—	V	*1
DCDC2 Line regulation	$DD2_{LINE}$	PV_{IN2} = 6 V to 24 V I_{OUT2} = 0.5 A	—	0.25	0.75	%/V	—
DCDC2 Load regulation	$DD2_{LOAD}$	I_{OUT2} = 10 mA to 6 A	—	3.5	—	%	*1
DCDC2 Output ripple voltage 1	$DD2_{RPL1}$	I_{OUT2} = 10 mA	—	40	—	mV [p-p]	*1
DCDC2 Output ripple voltage 2	$DD2_{RPL2}$	I_{OUT2} = 3 A	—	20	—	mV [p-p]	*1
DCDC2 Load transient response 1	$DD2_{TR1}$	I_{OUT2} = 100 mA to 3 A Δt = 0.5 A / µs	—	20	—	mV	*1
DCDC2 Load transient response 2	$DD2_{TR2}$	I_{OUT2} = 3 A to 100 mA Δt = 0.5 A / µs	—	20	—	mV	*1
DCDC2 High Side Power MOSFET ON resistance	$DD2R_{ONH}$	V_{GS} = 5.0 V	—	20	40	mΩ	—
DCDC2 Low Side Power MOSFET ON resistance	$DD2R_{ONL}$	V_{GS} = 5.0 V	—	20	40	mΩ	—
DCDC2 MIN input and output voltage difference	$DD2V_{diff}$	$DD2V_{diff} = PV_{IN2} - V_{OUT2}$	—	1.5	—	V	*1

Note: *1 : Typical Design Value.

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ELECTRICAL CHARACTERISTICS (Continued)

DCDC1 & DCDC2 : C_{OUT} = 22 µF × 4, L_{OUT} = 1 µH, V_{OUT} Setting = 1.1 V, V_{IN} = 12 V,
Switching Frequency = 600 kHz, T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
PROTECTION							
DC-DC1 Over Current Protection Limit	$DD1_{OCP}$	—	—	8.0	—	A	*1
DC-DC1 Short Circuit Protection Threshold	$DD1_{VSCP}$	V_{FB1} = 0.6 V to 0.0 V	50	60	70	%	—
DC-DC2 Over Current Protection Limit	$DD2_{OCP}$	—	—	8.0	—	A	*1
DC-DC2 Short Circuit Protection Threshold	$DD2_{VSCP}$	V_{FB2} = 0.6 V to 0.0 V	50	60	70	%	—
Thermal Shut Down (TSD) Threshold	TSD	—	—	130	—	°C	*1
Thermal Shut Down (TSD) Hysteresis	TSD_{HYS}	—	—	30	—	°C	*1
Soft Start Timing							
Soft start time DCDC1	$DD1_{SS}$	Δt = 90% V_{OUT1} -10% V_{OUT1}	—	0.8	—	ms	*1
Soft start time DCDC2	$DD2_{SS}$	Δt = 90% V_{OUT2} -10% V_{OUT2}	—	0.8	—	ms	*1
Switching Frequency							
Switching Frequency DCDC1	$DD1_{FREQ}$	I_{OUT1} = 3 A	—	600	—	kHz	*1
Switching Frequency DCDC2	$DD2_{FREQ}$	I_{OUT2} = 3 A	—	600	—	kHz	*1

Note: *1 : Typical Design Value.

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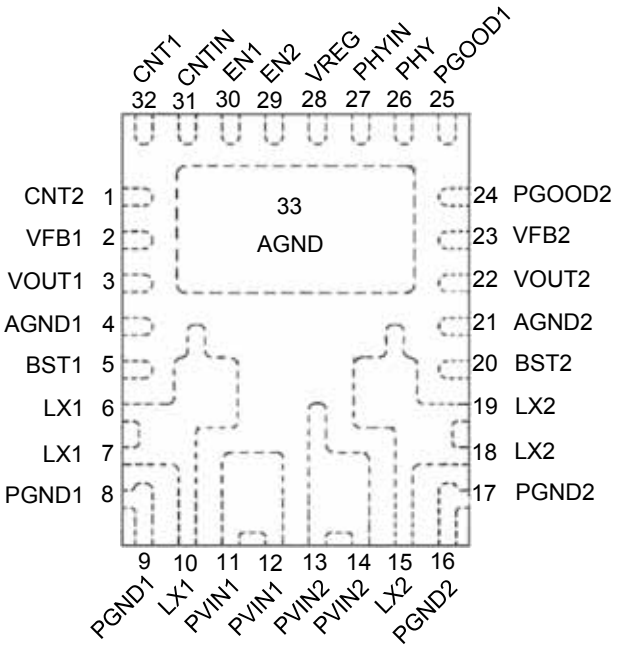
PIN CONFIGURATION

Top View



PIN FUNCTIONS

Pin No.	Pin name	Type	Description
1	CNT2	Output	Output to drive external MOSFET
2	VFB1	Input	Comparator negative input pin for DCDC 1 Or open connection for internal preset output voltage by internal feedback.
3	VOUT1	Input	Output voltage sense pin for DCDC 1
4	AGND1	Ground	Ground pin
5	BST1	Output	Supply input pin for high side FET gate driver for DCDC 1
6	LX1	Output	Power MOSFET output pin & for radiation of heat for DCDC 1
7			
10			
8	PGND1	Ground	Ground pin for Power MOSFET for DCDC 1
9			
11	PVIN1	Power supply	Power supply pin for Power MOSFET & for radiation of heat for DCDC 1
12			
13	PVIN2	Power supply	Power supply pin for Power MOSFET & for radiation of heat for DCDC 2
14			
16	PGND2	Ground	Ground pin for Power MOSFET for DCDC 2
17			
15	LX2	Output	Power MOSFET output pin & for radiation of heat for DCDC 2
18			
19			

Note: For the details on pin description, please refer to the OPERATION and APPLICATION INFORMATION section.

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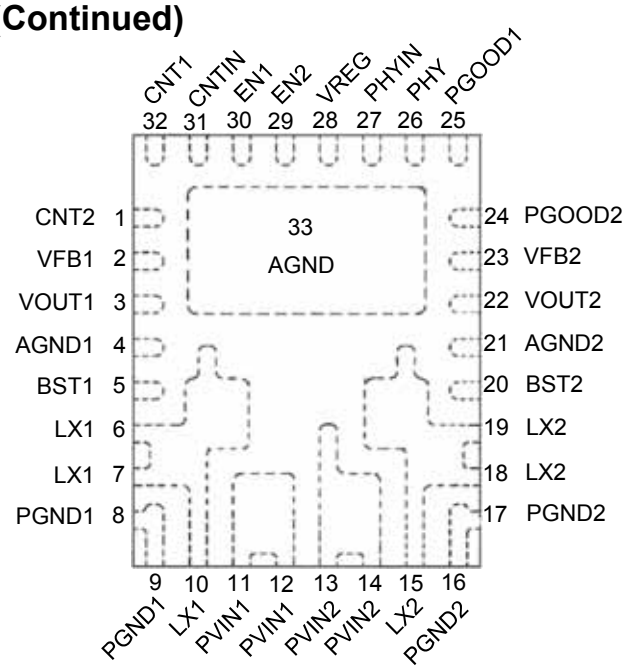
PIN CONFIGURATION (Continued)

Top View



PIN FUNCTIONS (Continued)

Pin No.	Pin name	Type	Description
20	BST2	Output	Supply input pin for high side FET gate driver for DCDC 2
21	AGND2	Ground	Ground pin
22	VOUT2	Input	Output voltage sense pin for DCDC 2
23	VFB2	Input	Comparator negative input pin for DCDC 2 Or open connection for internal preset output voltage by internal feedback.
24	PGOOD2	Output	Power good open drain pin for DCDC2 A pull up resistor between PGOOD 2 and VREG terminal is necessary. Output is low during Over or Under Voltage Detection conditions.
25	PGOOD1	Output	Power good open drain pin for DCDC1 A pull up resistor between PGOOD 1 and VREG terminal is necessary. Output is low during Over or Under Voltage Detection conditions.
26	PHY	Output	PHY LDO output pin (2.5V)
27	PHYIN	Power supply	PHY LDO supply input pin
28	VREG	Output	LDO output pin (5.5V)
29	EN2	Input	ON/OFF control pin for DCDC 2
30	EN1	Input	ON/OFF control pin for DCDC 1
31	CNTIN	Input	Pin to control CNT1 and CNT2
32	CNT1	Output	Output to drive external MOSFET
33	AGND	Output	Ground pad for heat radiation

Note : For the details on pin description, please refer to the OPERATION and APPLICATION INFORMATION section.

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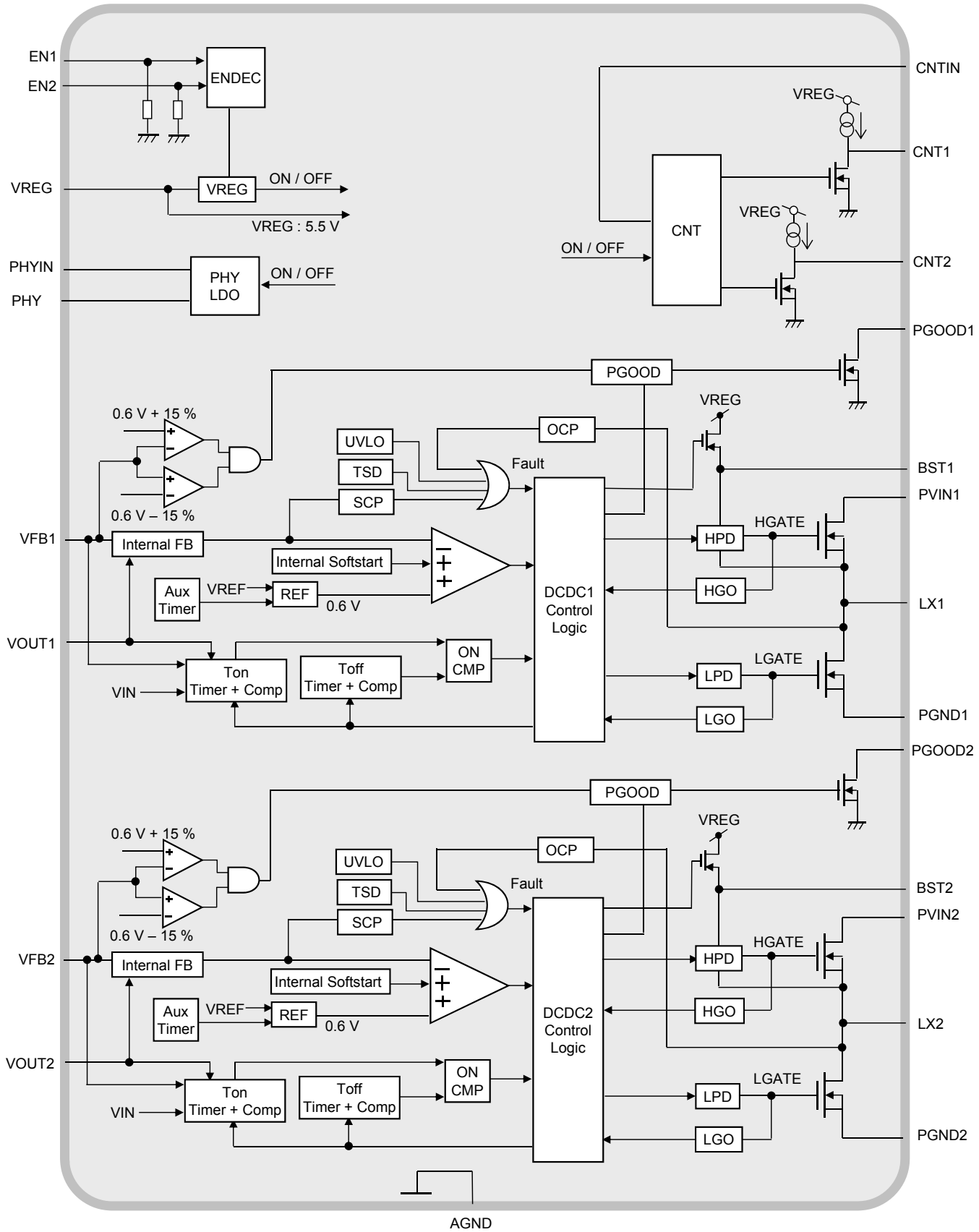
FUNCTIONAL BLOCK DIAGRAM



Note : This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

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OPERATION

1. Protection

(1) Over Current Protection (OCP) function and Short Circuit Protection (SCP) function

a) The Over Current Protection is activated at about 8 A (Typ). This device uses pulse-by-pulse valley current protection method. When the low side power MOSFET is turned on, the voltage across the drain and source is monitored which is proportional to the inductor current.

The high side power MOSFET is only allowed to turn on when the current flowing in the low side power MOSFET falls below the OCP level.

Hence, during the OCP, the output voltage continues to drop at the specified current. OCP is a non-latch type protection.

b) The Short Circuit Protection function is implemented when the output voltage decreases and the VFB1 (or VFB2) pin reaches to about 60 % of the set voltage (0.6 V). The SCP operates intermittently at about 2 ms ON, 16 ms OFF intervals.

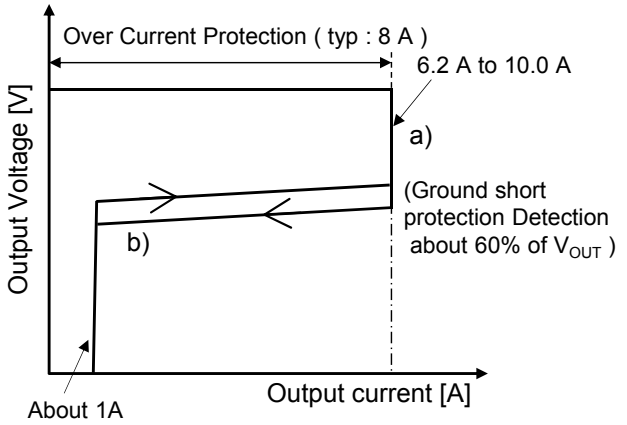

Figure 1-1 : OCP and SCP Operation

(2) Over Voltage Detection (OVD) and Under Voltage Detection (UVD)

a) The MOSFET connected to the PGOOD1 (or PGOOD2) pin turn ON when the output voltage rises and the VFB1 (or VFB2) pin voltage reaches 115 % of its set voltage (0.6 V).

b) After (a) above, the MOSFET connected to the PGOOD1 (or PGOOD2) pin is turned OFF after 1 ms when the output voltage drops and the VFB1 (or VFB2) pin voltage reaches 110 % of its set voltage (0.6 V).

c) The MOSFET connected to the PGOOD1 (or PGOOD2) pin turn ON when the output voltage drops and the VFB1 (or VFB2) pin voltage reaches 85 % of its set voltage (0.6 V).

d) After (c) above, the MOSFET connected to the PGOOD1(or PGOOD2) pin is turned OFF after 1 ms when the output voltage drops and the VFB1 (or VFB2) pin voltage reaches 90% of its set voltage (0.6 V).

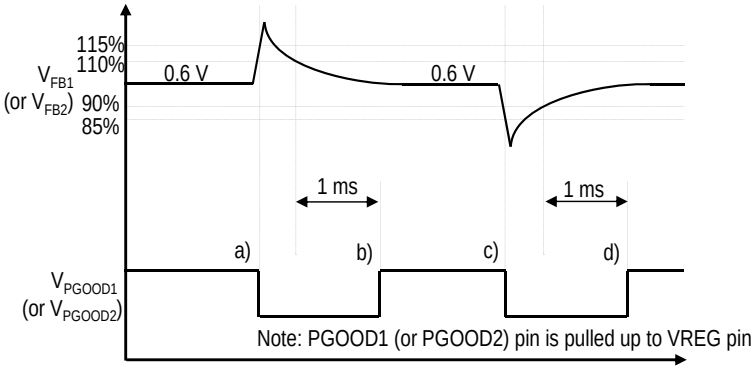

Figure 1-2 : OVD and UVD Operation

(3) Output discharging function

When EN1 (or EN2) is low, the output 1 (or output 2) is discharged by an internal MOSFET that is connected to VOUT1 (or VOUT2) pin.
When EN1 (or EN2) is high, if the controller is turned off by Under Voltage Lock Out (UVLO), the output 1 (output 2) is also discharged by the above said internal MOSFET. The on resistance of the internal MOSFET is about 50 Ω.

(4) Thermal Shut Down (TSD)

When the IC internal temperature becomes more than about 130°C, TSD operates and DC-DC turns off.

Established : 2014-03-19
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OPERATION (Continued)

2. Output Voltage Setting

(1) External feedback

The Output Voltage can be set by external resistance of FB pin, and its calculation is as follows.

$$V_{OUT} = \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \times 0.6$$

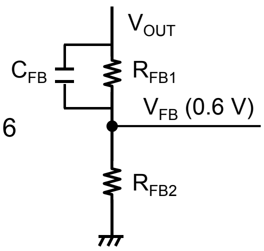

Figure 2-1 : External feedback

Below resistors are recommended for following popular output voltages.

VOUT [V]	RFB1 [Ω]	RFB2 [Ω]
5.00	88 k	12 k
3.30	54 k	12 k
2.85	75 k	20 k
1.80	36 k	18 k
1.10	15 k	18 k
1.00	12 k	18 k

RFB2 has to be ≤ 20kΩ to avoid triggering the internal feedback function.

Also, if you set the V_{OUT} > 1.8V, it is recommended to use the C_{FB} between VOUT and VFB of 1nF.

VFB comparator threshold is adjusted to ± 1 %, but the actual output voltage accuracy becomes more than ± 1 % due to the influence from the circuits other than VFB comparator.

In the case of V_{OUT} setting = 3.3 V, the actual output voltage accuracy becomes ± 2.5 %.
(V_{IN} = 12 V, I_{OUT} = 3 A).

(2) Internal feedback (Preset output voltage)

This IC has built-in feedback resistors with preset output voltage at 1.1V. If VFB1 (or VFB2) pin is floating at the timing of EN1 (or EN2) going from Low to High, the internal feedback function will be activated.

Using CFB with internal feedback is possible but the CFB has to be ≤ 250pF.

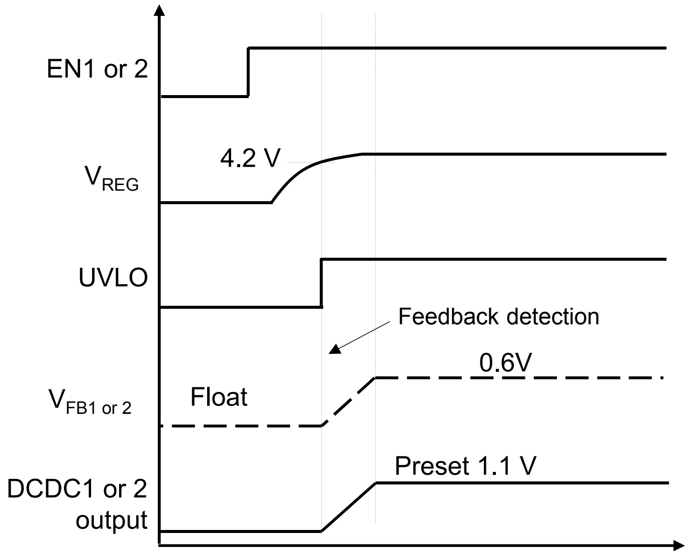

Figure 2-2 : Internal feedback operation

3. Soft Start

This IC has build-in Soft Start function without using external component. Soft Start function maintains the smooth control of the output voltage during start up to avoid overshoot & rush current.

When the EN1 (or EN2) pin becomes High, the DCDC1 (or DCDC2) output voltage rise up in the period of about 1ms with the tolerance of 30%.

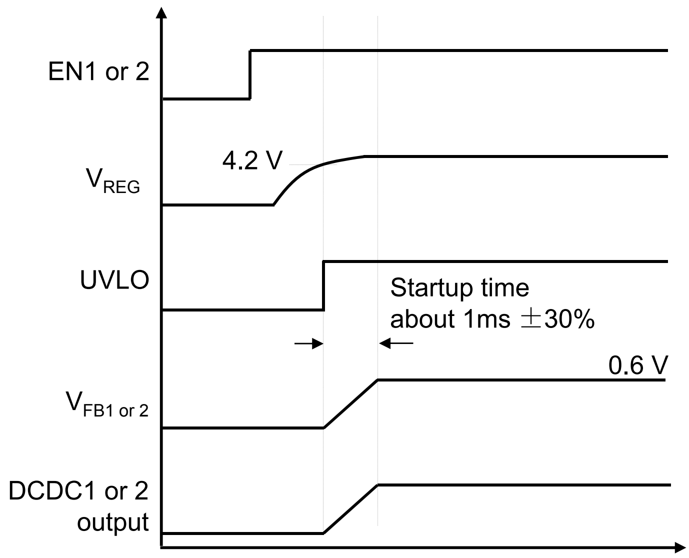

Figure 2-3 : Soft Start (SS) Operation

OPERATION (Continued)

4. Internal regulators

This IC has 2 internal regulators which are enabled/ disabled by either EN1 or EN2.

External capacitors should be placed near the VREG, PHYIN and PHY pins for stable operation.

(1) VREG

The voltage of VREG pin regulator is 5.5V and it is used to supply internal circuits of IC. The VREG has current capability of about 100mA and has over-current protection.

(2) PHY

The voltage of PHY regulator is 2.5V and current capability is about 100mA (PHYIN=5V). The PHYIN can be connected to any external voltage source which is between 3V to 5.5V.

The PHY also has over-current protection.

5. EN & CNT Settings

(1) EN1 and EN2

The Start up / Shut down is enabled by the EN1 or EN2 pin. The EN1 controls DCDC1 and EN2 controls DCDC2. Both EN are able to control internal regulators VREG and PHY regulator.

The EN1 and EN2 pin input voltage (V_{ENH}, V_{ENL}) should satisfy the conditions as defined in the electrical characteristics.

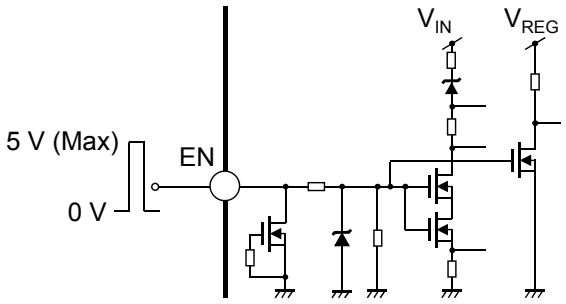

Figure 5-1 : Internal circuit with EN pin

(2) CNTIN, CNT1 & CNT2

CNTIN is the input control for CNT1 and CNT2. Two input control signals from external system are combined into CNTIN pin by 2 external resistors.

CNTIN detects the voltage level and decide the CNT1 and CNT2 output condition.

CNTIN becomes active only when either EN1 or EN2 is enabled.

The high-level voltage of control signals (INCNT1& INCNT2) should be 1.8V and above.

CNT1 and CNT2 have around 1uA of sourcing current to make softstart effect on the gate of external MOSFET.

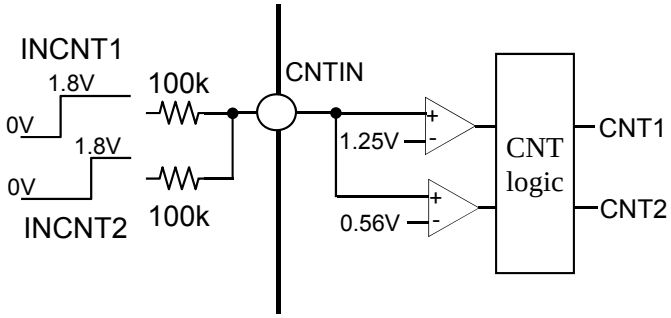

Figure 5-2 : CNTIN, CNT1 & CNT2 circuit

Below are the input & output combination.

From external		CNTIN Pin	CNT1	CNT2
INCNT1	INCNT2			
0V	0V	0V	0V	0V
1.8V	0V	0.9V	5.5V	0V
1.8V	1.8V	1.8V	5.5V	5.5V

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OPERATION (Continued)

6. Power ON / OFF Sequence

(1) When the EN1 or EN2 pin is set to High after the V_{IN} settles, the BGR and the VREG started up.

(2) When the VREG pin exceeds its threshold value, the UVLO is released. The internal Soft-Start (SS) sequence is enabled. Also, the PHY output is started up, CNT1 and CNT2 are activated.

(3) The VOUT1 or VOUT2 pin (DC-DC Output) voltage increases at the same rate as the internal SS. Normal operation begins after the VOUT1 or VOUT2 pin reaches the set voltage.

(4) When both the EN pin are set to Low, the BGR, VREG and UVLO stop operation.

The VOUT1 and VOUT2 pin voltage starts to drop and the discharge time depends on the value of the feedback resistors, the output load current and output capacitors.

The PHY, CNT1 and CNT2 also stop operation when both EN1 and EN2 are set to low together.

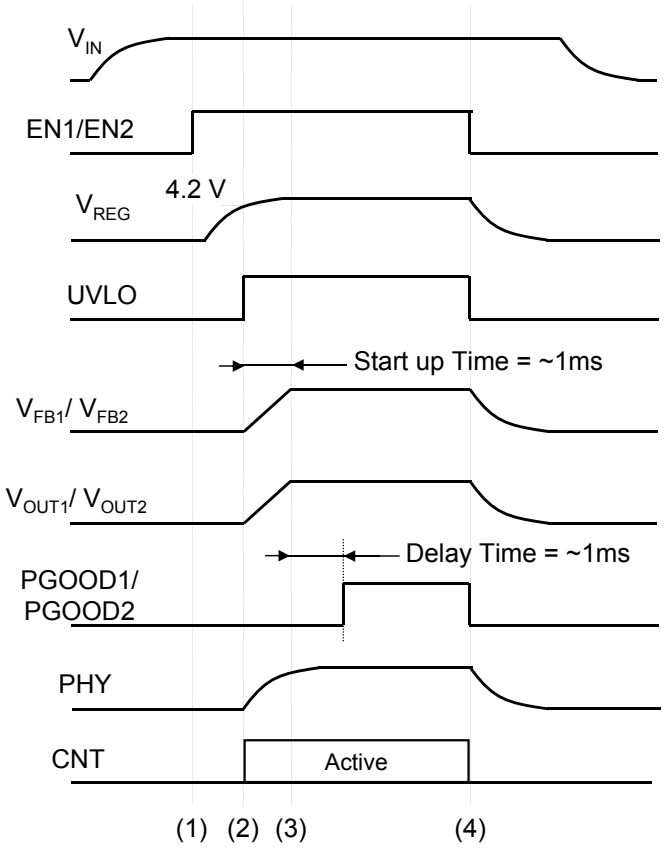

Figure 6-1 : Power ON/OFF sequence

(5) Referring to the Figure below, for the condition when V_{IN} voltage is decreasing while EN1 or EN2 is still high, output voltage (V_{OUT1}/V_{OUT2}) can maintain at the set voltage level prior to UVLO detection voltage (UVLO detection is about 3.8V).

For this operation to be valid, please note that the set voltage level at the output (V_{OUT1}/V_{OUT2}) is lower than the UVLO detection voltage with consideration of the output (V_{OUT1}/V_{OUT2}) dropout voltage from V_{IN}.

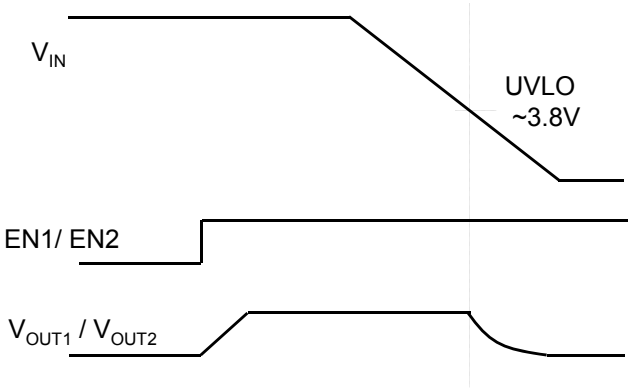

Figure 6-2 : V_{IN} power down sequence

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OPERATION (Continued)

7. Inductor and Output Capacitor Setting

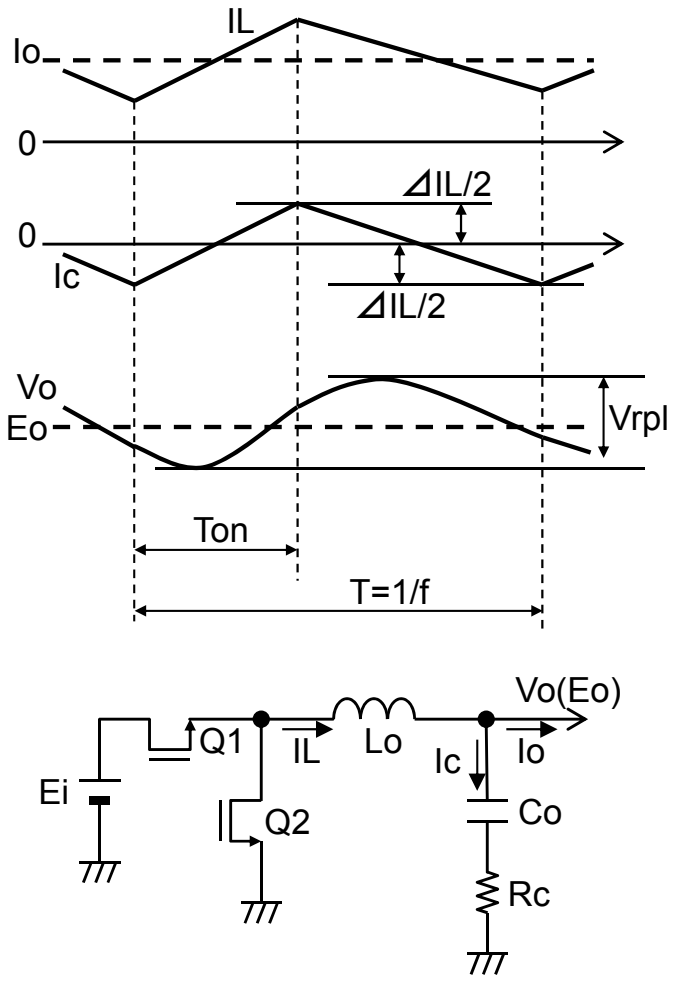

Figure 7-1 : Output ripple for output inductor and capacitor

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current.

$$\Delta IL = \frac{Eo \cdot (Ei - Eo)}{Ei \cdot Lo \cdot f}$$

$$Iox = \frac{\Delta IL}{2}$$

Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade off among component size, efficiency and operating frequency. A reasonable starting point is to choose a ripple current that is about 40 % of I_O (MAX). The largest ripple current occurs at the highest Ei. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$Lo \geq \frac{Eo \cdot (Ei - Eo)}{2Ei \cdot Iox \cdot f} \quad @\ \mathrm{Ei} = \mathrm{Ei\_max}$$

And its maximum current rating is

$$IL\_\max = \mathrm{Io\_max} + \frac{\Delta IL}{2} \quad (@\ \mathrm{Ei} = \mathrm{Ei\_max})$$

The selection of Co is primarily determined by the ESR (Rc) required to minimize voltage ripple and load transients. The output ripple Vrpl is approximately bounded by:

$$Vrpl = Vop - Vob = Ei \cdot \frac{Co \cdot Rc^2}{2Lo} + \frac{\Delta IL}{8Co \cdot f}$$

$$= Ei \cdot \frac{Co \cdot Rc^2}{2Lo} + \frac{Eo \cdot (Ei - Eo)}{8Ei \cdot Lo \cdot Co \cdot f^2}$$

From the above equation, to achieve desired output ripple, low ESR ceramic capacitors are recommended, and its required RMS current rating is:

$$Ic(\mathrm{rms})\_\max = \frac{\Delta IL}{2\sqrt{3}} \quad (@\ \mathrm{Ei} = \mathrm{Ei\_max})$$

Established : 2014-03-19
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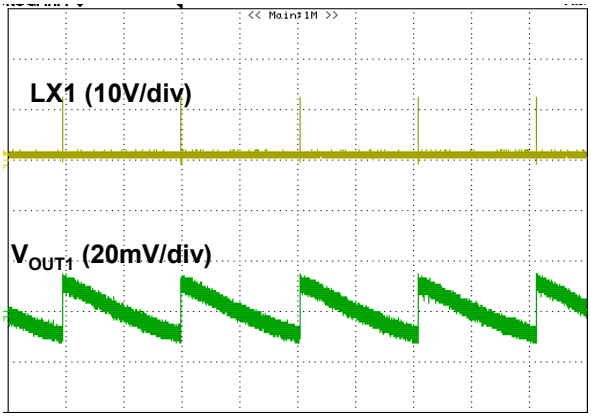
TYPICAL CHARACTERISTICS CURVES

1. Output Ripple Voltage

Condition : V_{IN} = 12 V, V_{OUT1} = 1.1 V, L_{OUT1} = 1 µH, C_{OUT1} = 88 µF (22 µF x 4)

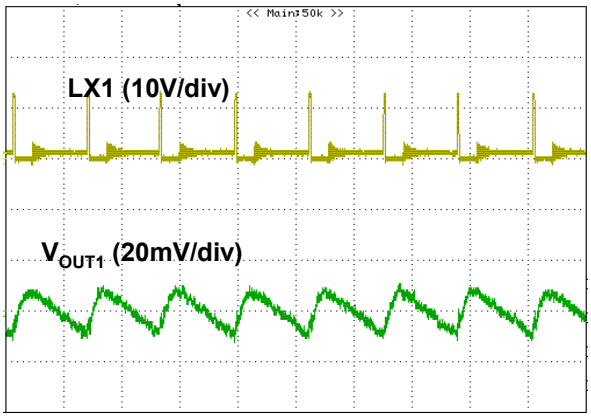
Characteristic 1-1

I_{OUT1} = 0 A



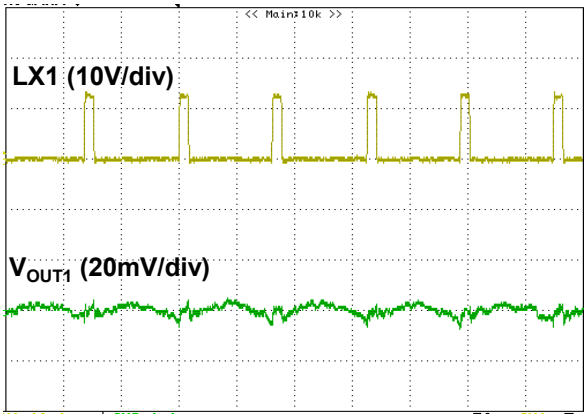
Characteristic 1-2

I_{OUT1} = 0.2 A



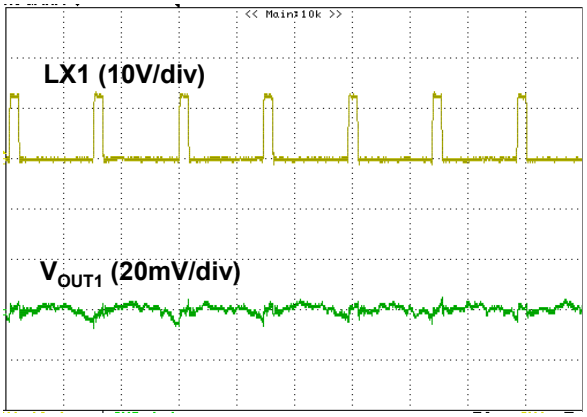
Characteristic 1-3

I_{OUT1} = 3 A



Characteristic 1-4

I_{OUT1} = 6 A



Established : 2014-03-19
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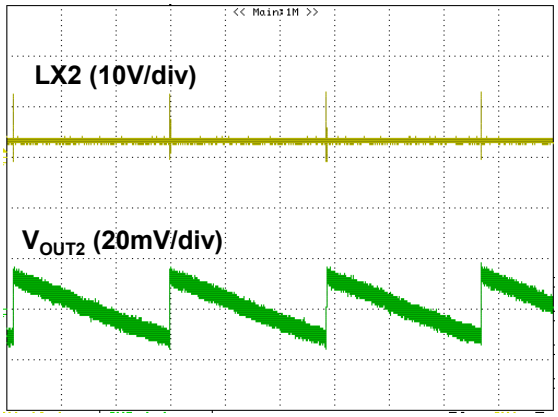
TYPICAL CHARACTERISTICS CURVES (Continued)

1. Output Ripple Voltage (Continued)

Condition : V_{IN} = 12 V, V_{OUT2} = 3.3 V, L_{OUT2} = 2.2 µH, C_{OUT2} = 88 µF (22 µF x 4)

Characteristic 1-5

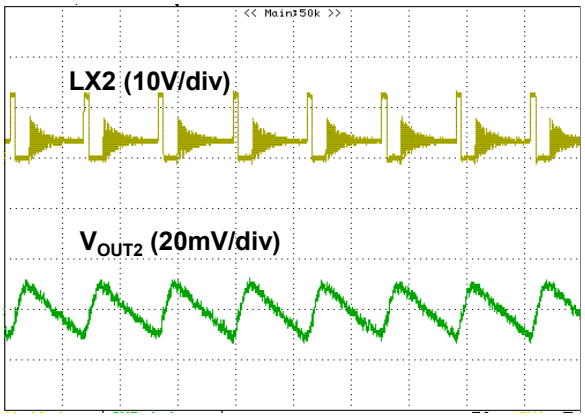
I_{OUT2} = 0 A



TIME (5ms/div)

Characteristic 1-6

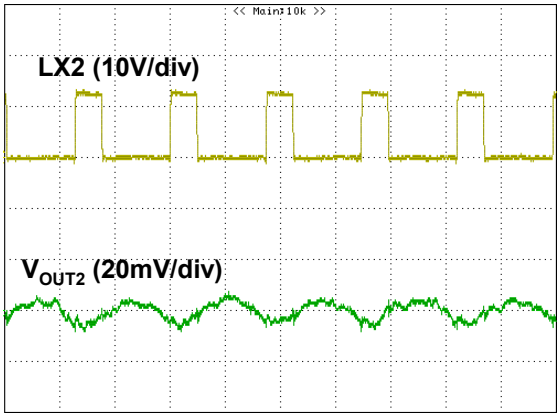
I_{OUT2} = 0.2 A



TIME (5us/div)

Characteristic 1-7

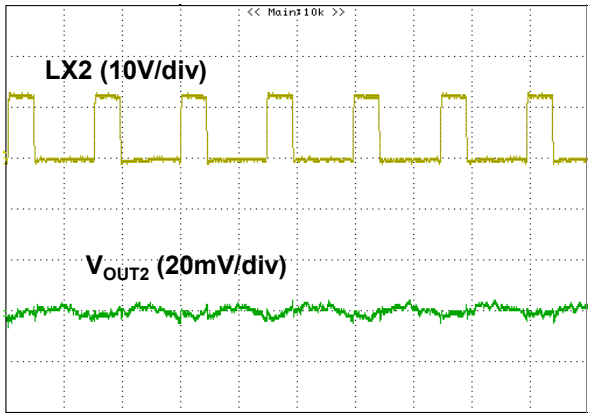
I_{OUT2} = 3 A



TIME (1us/div)

Characteristic 1-8

I_{OUT2} = 6 A



TIME (1us/div)

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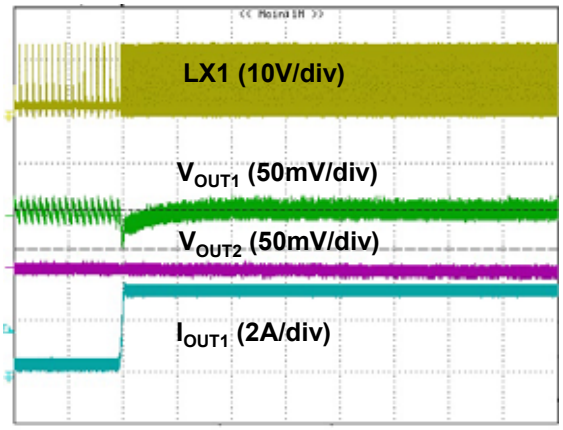
TYPICAL CHARACTERISTICS CURVES (Continued)

2. Load transient response

Condition : V_{IN} = 12 V, V_{OUT1} = 1.1 V, V_{OUT2} = 3.3 V, L_{OUT1} = 1 µH, L_{OUT2} = 2.2 µH, C_{OUT} = 88 µF (22 µF x 4)

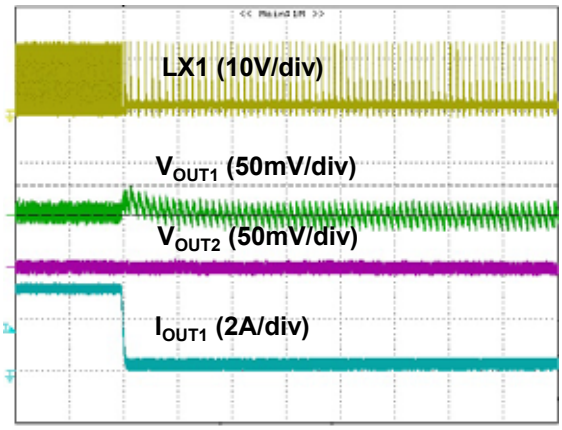
Characteristic 2-1

Load transient on V_{OUT1} , V_{OUT1} = 1.1 V



I_{OUT1} = 100 mA to 3A (0.5A/µs)
V_{OUT1} undershoot less than 50 mV
V_{OUT2} is stable.

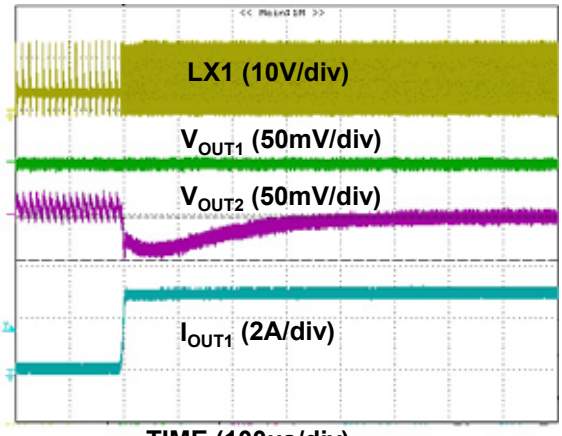
Characteristic 2-2



I_{OUT1} = 3 A to 100 mA (0.5A/µs)
V_{OUT1} overshoot less than 50 mV
V_{OUT2} is stable.

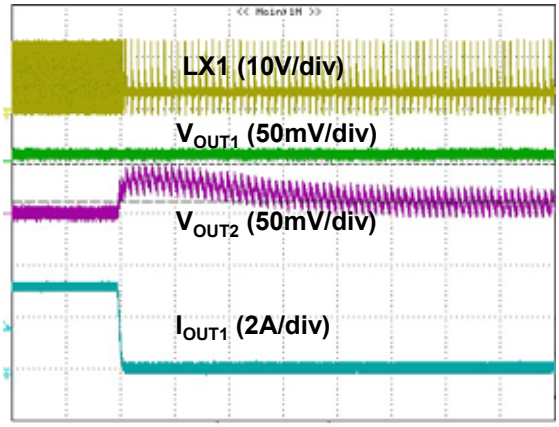
Characteristic 2-3

Load transient on V_{OUT2} , V_{OUT2} = 3.3 V



I_{OUT2} = 100 mA to 3A (0.5A/µs)
V_{OUT2} undershoot less than 50 mV
V_{OUT1} is stable.

Characteristic 2-4



I_{OUT2} = 3 A to 100 mA (0.5A/µs)
V_{OUT2} overshoot less than 50 mV
V_{OUT1} is stable.

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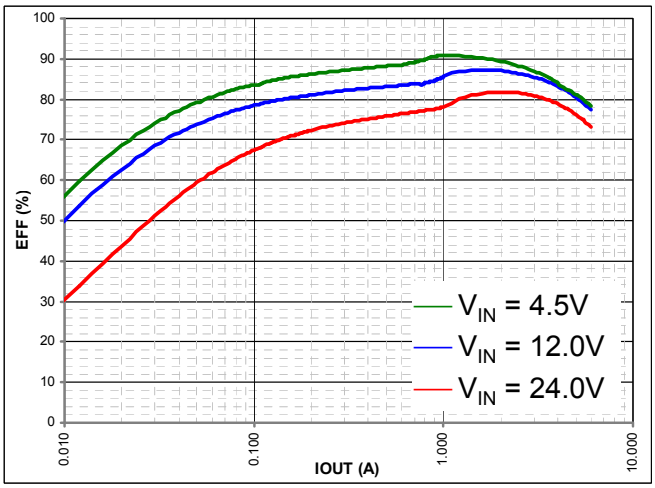
TYPICAL CHARACTERISTICS CURVES (Continued)

3. Efficiency

Condition : L_{OUT} = 1 µH / 2.2 µH / 3.3 µH, C_{OUT} = 88 µF (22 µF x 4)

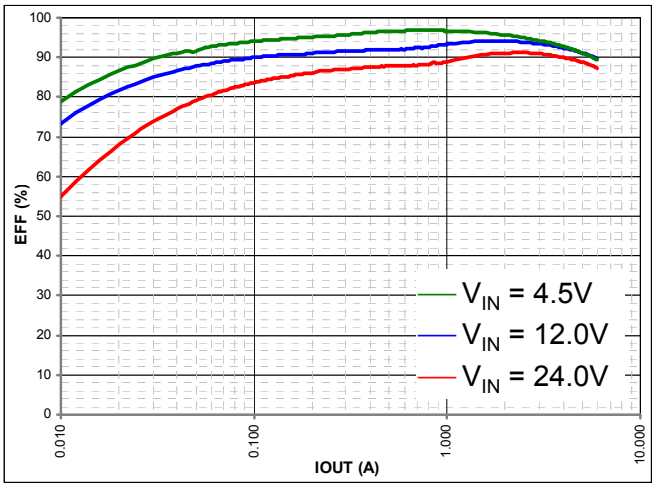
Characteristic 3-1

V_{OUT} = 1.1 V,
L_{OUT}=1µH



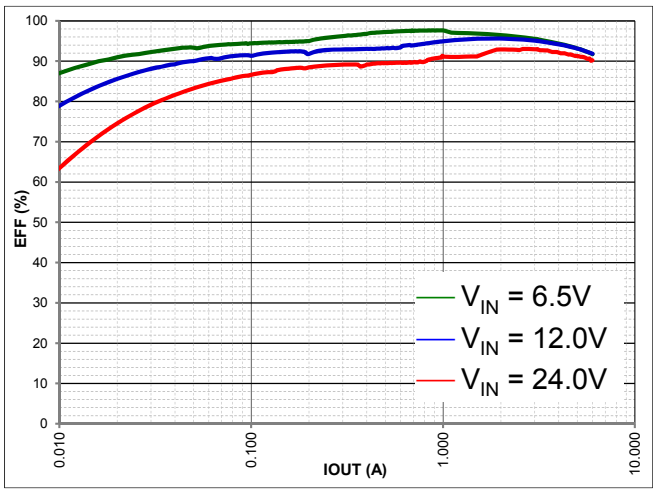
Characteristic 3-2

V_{OUT} = 3.3 V,
L_{OUT}=2.2µH



Characteristic 3-3

V_{OUT} = 5.0 V,
L_{OUT}=3.3µH



Established : 2014-03-19
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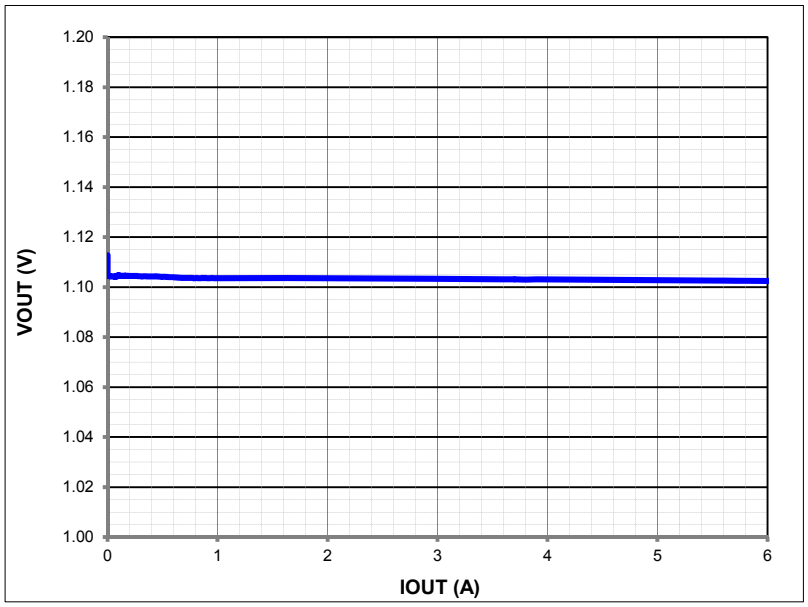
TYPICAL CHARACTERISTICS CURVES (Continued)

4. Load Regulation

Condition : V_{IN} = 12 V, L_{OUT1} = 1 µH, L_{OUT2} = 2.2 µH, C_{OUT} = 88 µF (22 µF x 4)

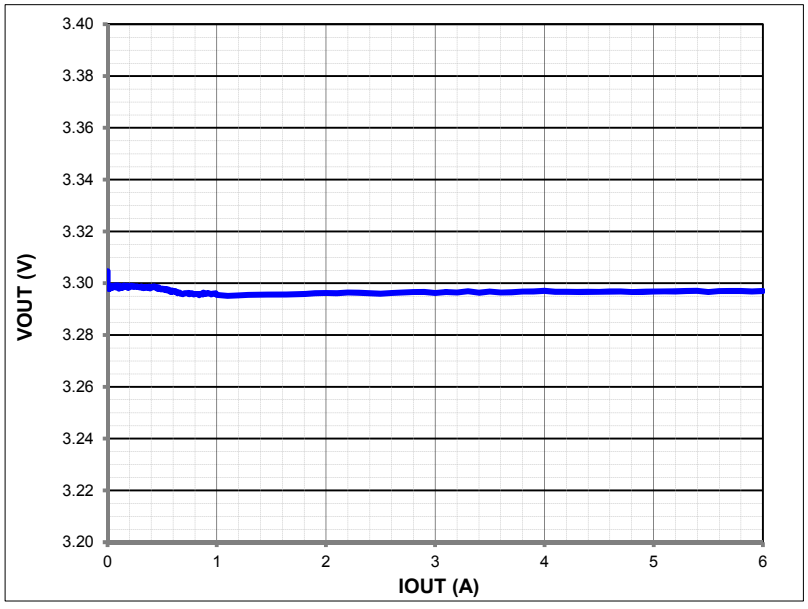
Characteristic 4-1

V_{OUT1} = 1.1 V



Characteristic 4-2

V_{OUT2} = 3.3 V



Established : 2014-03-19
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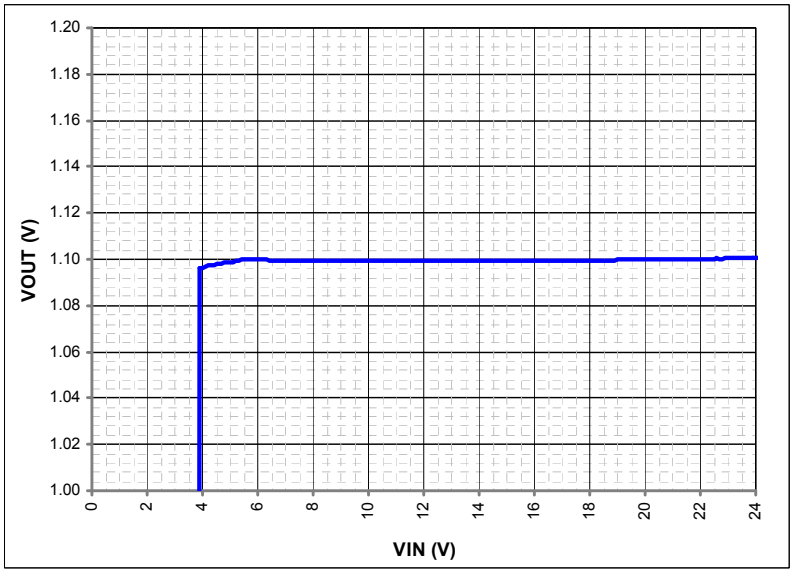
TYPICAL CHARACTERISTICS CURVES (Continued)

5. Line Regulation

Condition : V_{IN} = 12 V, I_{OUT} = 3 A, L_{OUT1} = 1 µH, L_{OUT2} = 2.2 µH, C_{OUT} = 88 µF (22 µF x 4)

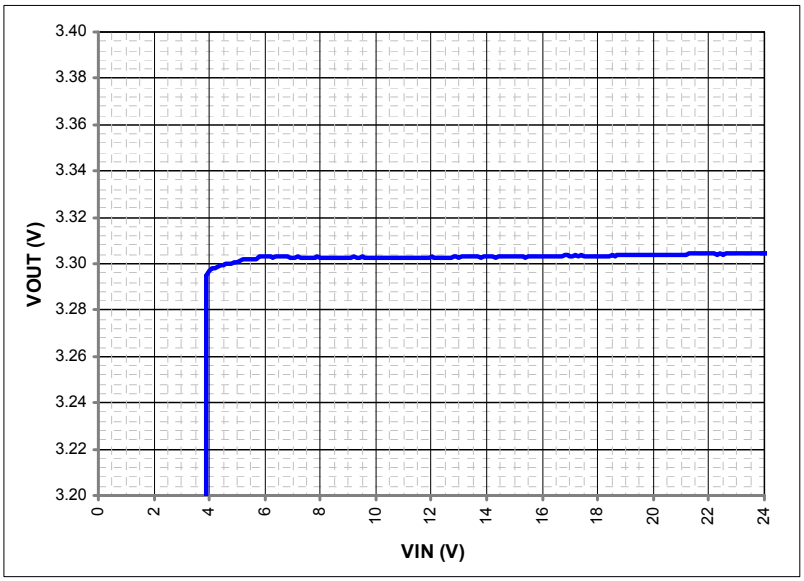
Characteristic 5-1

V_{OUT1} = 1.1 V



Characteristic 5-2

V_{OUT2} = 3.3 V



Established : 2014-03-19
Revised : 2015-01-17

TYPICAL CHARACTERISTICS CURVES (Continued)

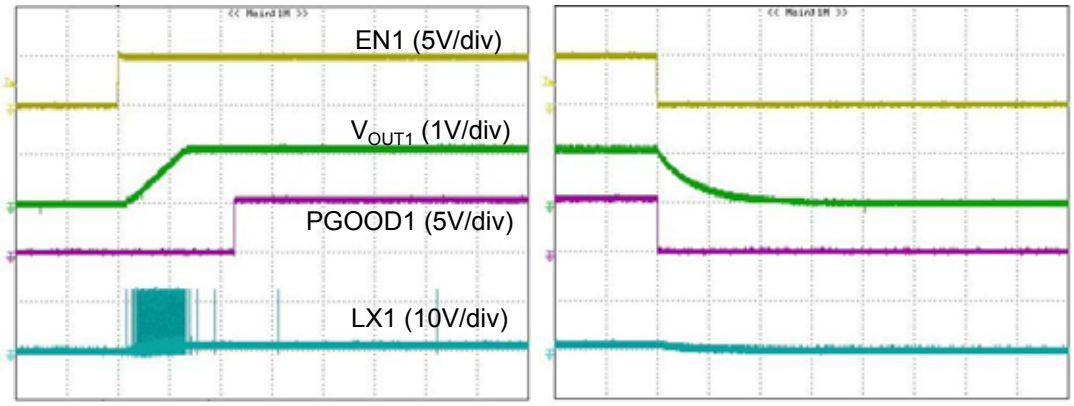
6. Start / Shut Down

Condition : V_{IN} = 12 V, V_{OUT1} = 1.1 V, V_{OUT2} = 1.8 V, L_{OUT1} = 1 µH, L_{OUT2} = 1 µH, C_{OUT} = 88 µF (22 µF x 4)

Characteristic 6-1

Enable V_{OUT1} only

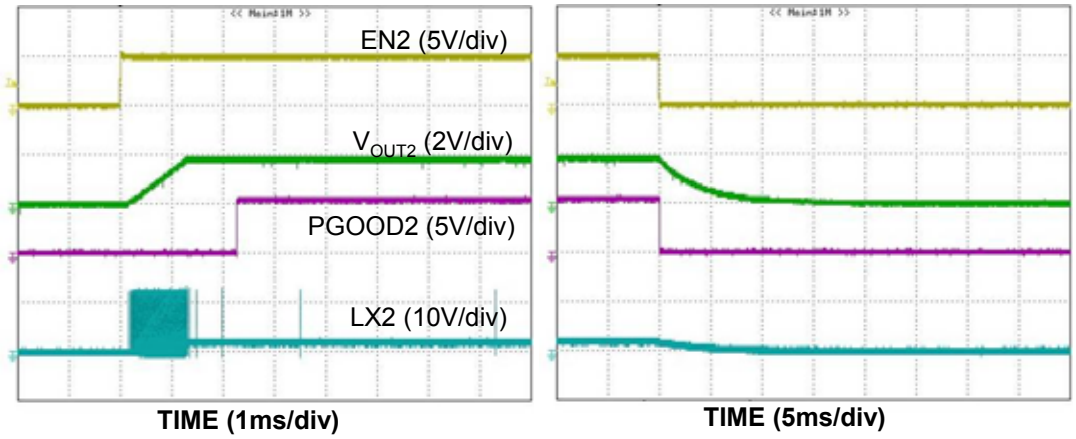
Characteristic 6-2



Characteristic 6-3

Enable V_{OUT2} only

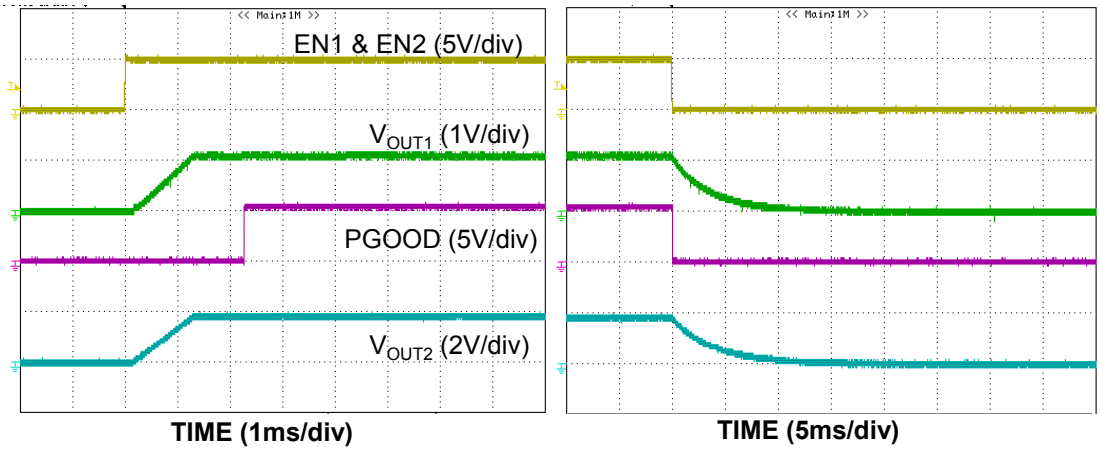
Characteristic 6-4



Characteristic 6-5

Enable V_{OUT1} & V_{OUT2}

Characteristic 6-6



Established : 2014-03-19
Revised : 2015-01-17

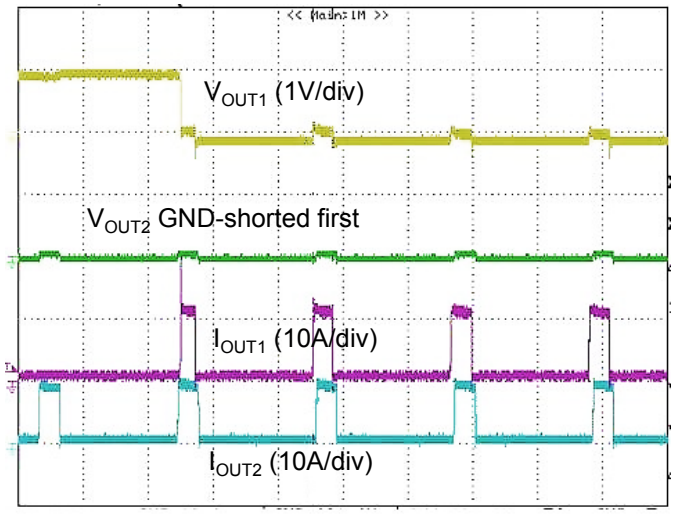
TYPICAL CHARACTERISTICS CURVES (Continued)

7. Short Circuit Protection

Condition : V_{IN} = 12 V, V_{OUT1} = 1.1 V, V_{OUT2} = 3.3 V, L_{OUT1} = 1 µH, L_{OUT2} = 2.2 µH, C_{OUT} = 88 µF (22 µF x 4)

Characteristic 7-1

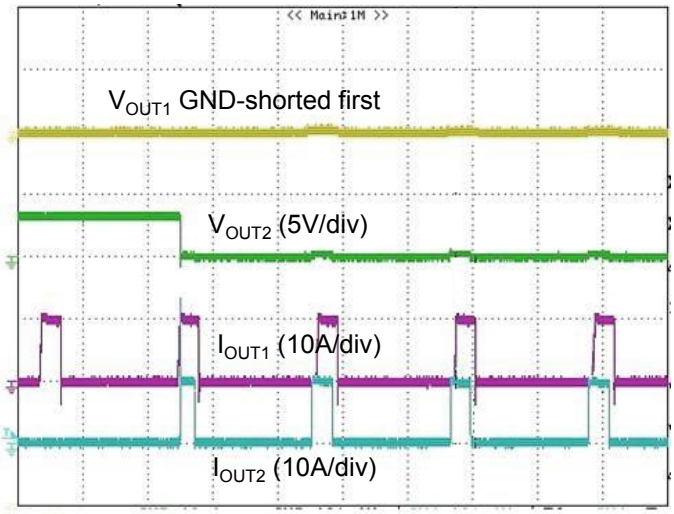
While V_{OUT2} is still in SCP, V_{OUT1} is shorted



TIME (10ms/div)

Characteristic 7-2

While V_{OUT1} is still in SCP, V_{OUT2} is shorted



TIME (10ms/div)

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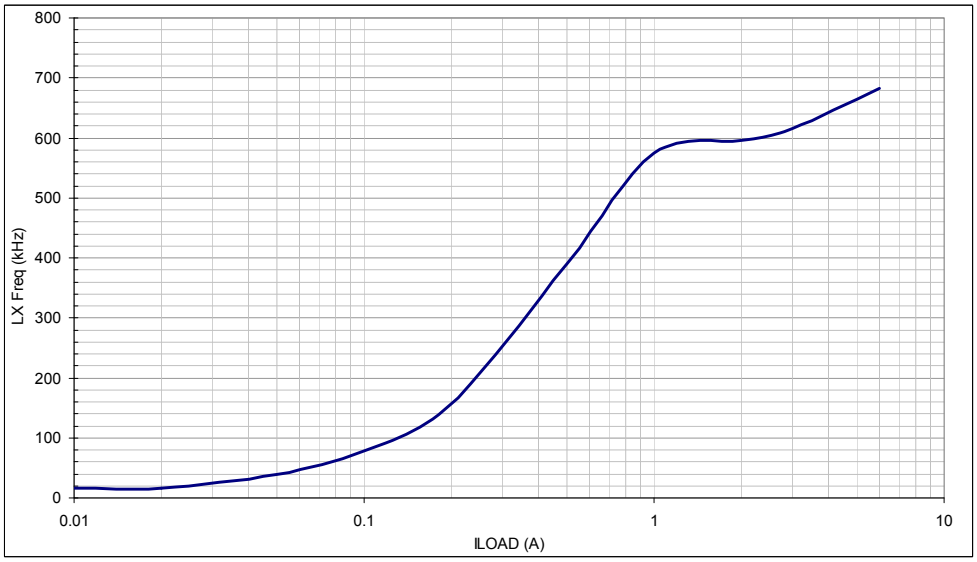
TYPICAL CHARACTERISTICS CURVES (Continued)

8. Switching Frequency

Condition : V_{IN} = 12 V, L_{OUT1} = 1 µH, L_{OUT2} = 2.2 µH, C_{OUT} = 88 µF (22 µF x 4)

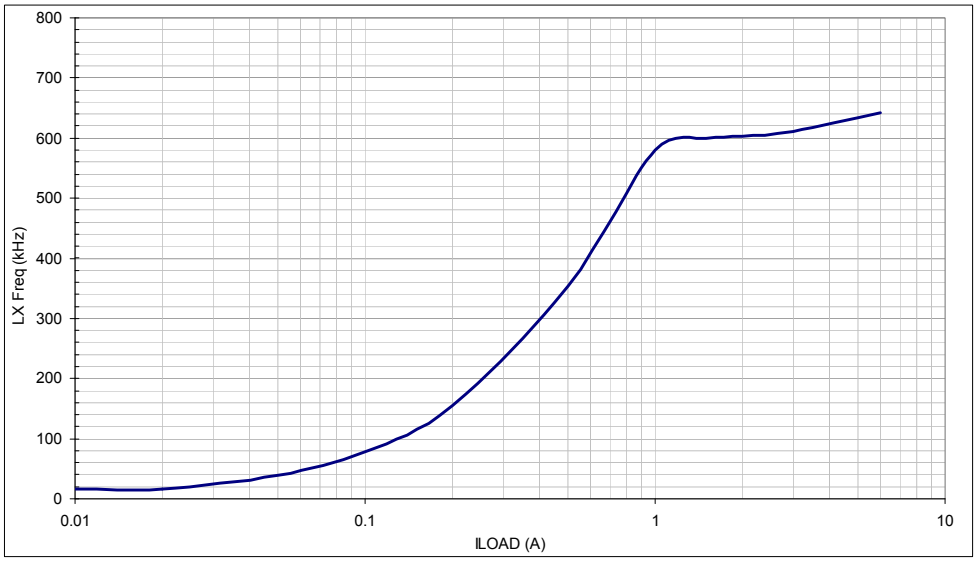
Characteristic 8-1

V_{OUT1} = 1.1 V



Characteristic 8-2

V_{OUT2} = 3.3 V



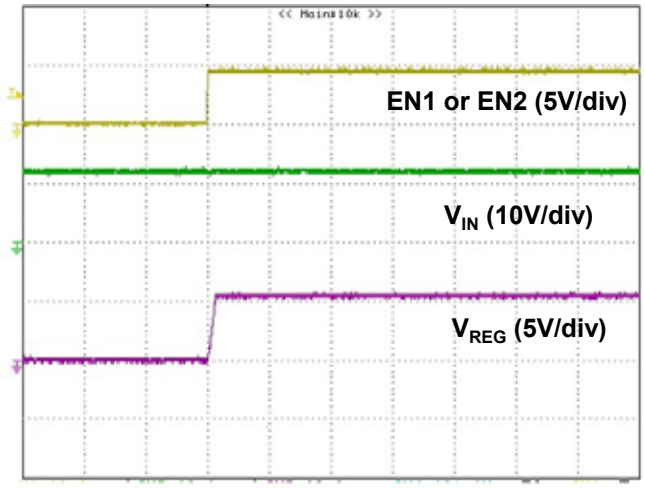
Established : 2014-03-19
Revised : 2015-01-17

TYPICAL CHARACTERISTICS CURVES (Continued)

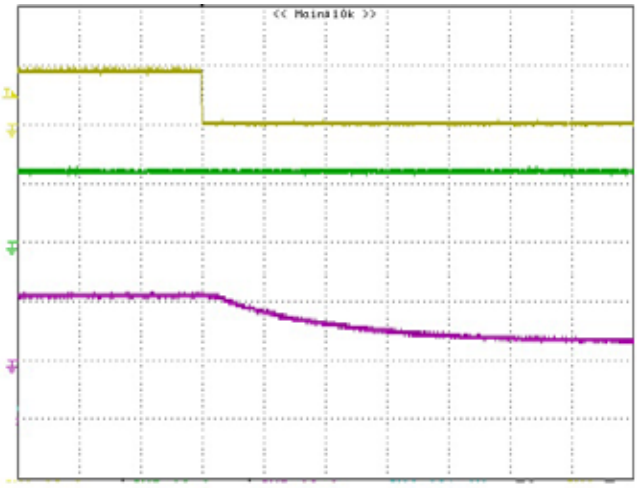
9. VREG and PHY LDO Start / Shut Down

Condition : V_{IN} = 12 V, C_{VREG} = 4.7 µF, C_{PHYIN} = 1 µF, C_{PHY} = 1 µF

Characteristic 9-1

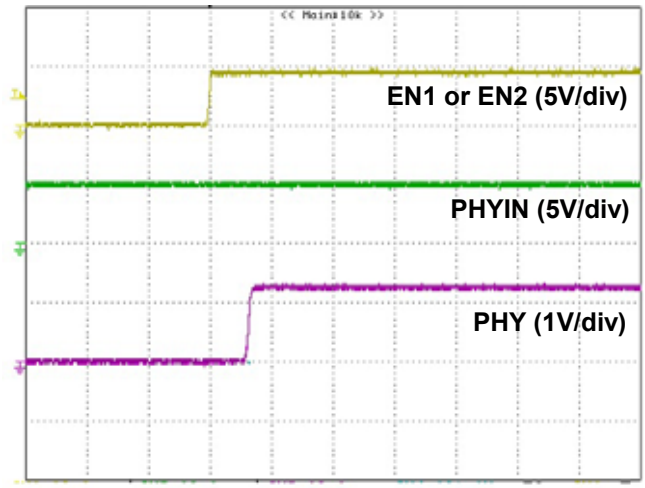


Characteristic 9-2

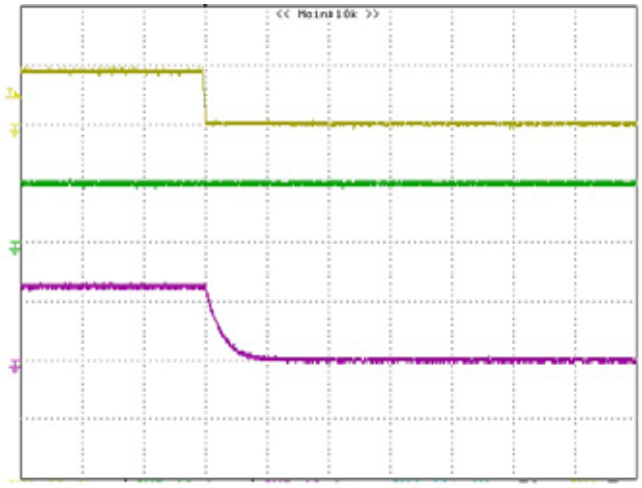


TIME (1ms/div)

Characteristic 9-3



Characteristic 9-4



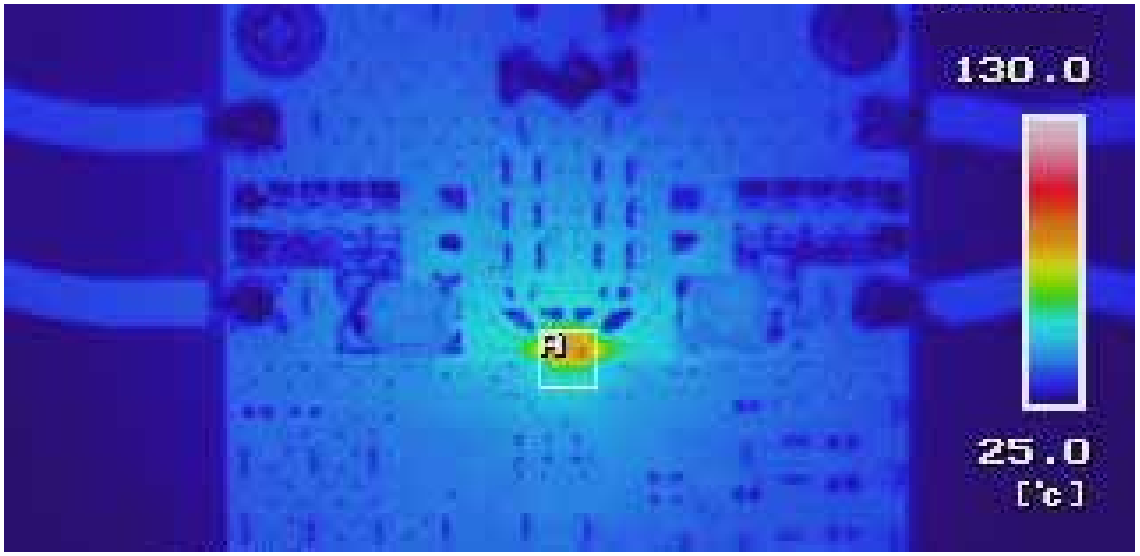
TIME (200us/div)

Established : 2014-03-19
Revised : 2015-01-17

TYPICAL CHARACTERISTICS CURVES (Continued)

10. Thermal Performance and Safe Operation Area

Condition : V_{IN} = 12 V, V_{OUT1} = 1.1 V, V_{OUT2} = 1.1 V, I_{OUT1} = 5A, I_{OUT2} = 5A, L_{OUT} = 1 µH, C_{OUT} = 88 µF (22 µF x 4)



IC case temperature is about 70 ° C

Figure 10-1 : Thermal image

This IC is intended to be used for general electronic equipment. Ensure that the IC is used within the recommended safe operating region illustrated by the reference graph on the right. Do take note that thermal performance may varies with PCB design and PCB materials.
Please use the graph only as a reference for your design and discuss further with our application engineer.
It is to be understood that our company shall not be held responsible for any damage incurred as a result of application beyond the recommended safe operating region.

Recommended Safe Operation Area for VOUT from 1V to 5V with the condition of casing surface temperature below 85°C.

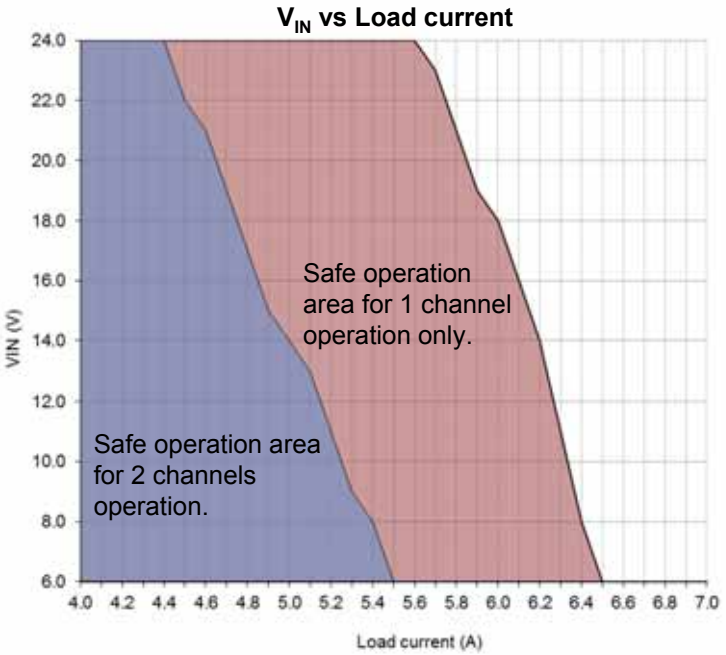


Figure 10-2 : Reference Safe Operation Area

Established : 2014-03-19
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APPLICATIONS INFORMATION

1. Evaluation Board Information

Condition : V_{IN} = 12 V, V_{OUT1} = 1.1 V, V_{OUT2} = 3.3 V, L_{OUT1} = 1 µH, L_{OUT2} = 2.2 µH, C_{OUT} = 88 µF (22 µF x 4)

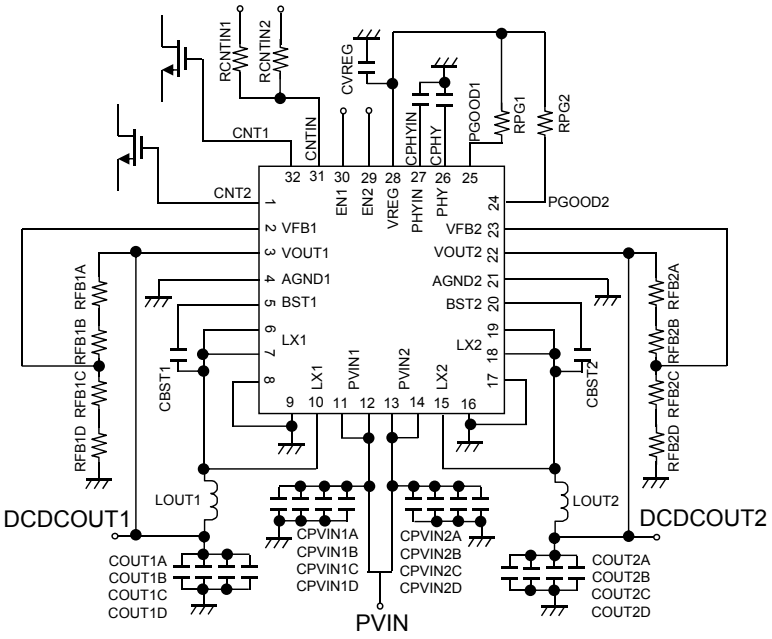

Figure A1-1 : Application circuit

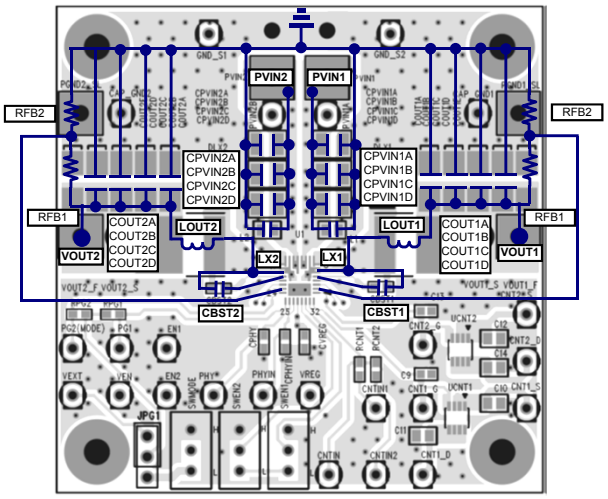

Figure A1-2 : Layout

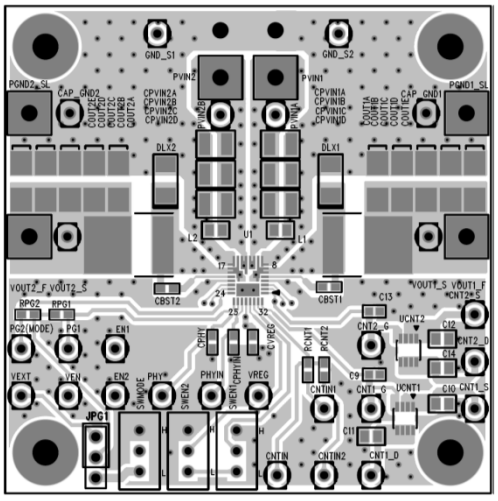

Figure A1-3 : Top Layer with silk screen
(Top View) with Evaluation board

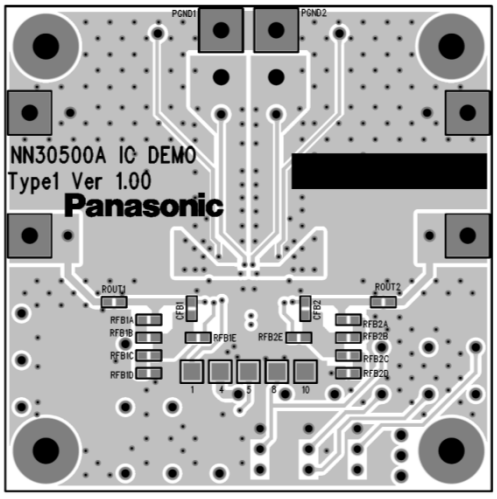

Figure A1-4 : Bottom Layer with silk screen
(Bottom View) with Evaluation board

Note: The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

Established : 2014-03-19
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APPLICATIONS INFORMATION (Continued)

2. Layout Recommendations

Board layout considerations are necessary for stable operation of the DC-DC regulator. The following precautions must be used when designing the board layout.

(a) The Input capacitor C_{IN} must be placed in such a way that the distance between PVIN and PGND is minimum, in order to suppress the switching noise. Stray inductance and impedance should be reduced as indicated by loop (1) in the figure below.

(b) A single point ground connection (2) must be used to connect PGND and AGND to improve operation stability.

(c) Output current line I_{OUT} and the output sense line VOUT must have small common impedance to reduce output load variations. Output sense line VOUT must be close to the output condenser C_{OUT} as indicated by (3) below.

(d) Power Loss and output ripple voltage can be reduced by placing the inductor L_{OUT} and output capacitor C_{OUT} such that the stray inductance and the impedance of loop (4) is minimum.
This is realized by :
i) Minimizing distance between inductor L_{OUT} and LX pin.
ii) Reducing distance between output capacitor C_{OUT} and (2) / (3).

(e) Thick lines in the application circuit example represent lines with large current flow. These lines should be designed as thick as possible.

(f) VFB / VREG lines should be placed far away from LX line, BST line and inductor L_{OUT} to reduce the effects of switching noise. These lines should be designed as short as possible. This is especially true for the VFB line, which is a high impedance line.

(g) R_{FB1} / R_{FB2} should also be placed as far away as possible from LX line, BST line and inductor L_{OUT} to minimize the effects of switching noise. R_{FB1} / R_{FB2} should be placed close to the VFB pin.

(h) LX / BST lines are noisy lines. They should be designed as short as possible.

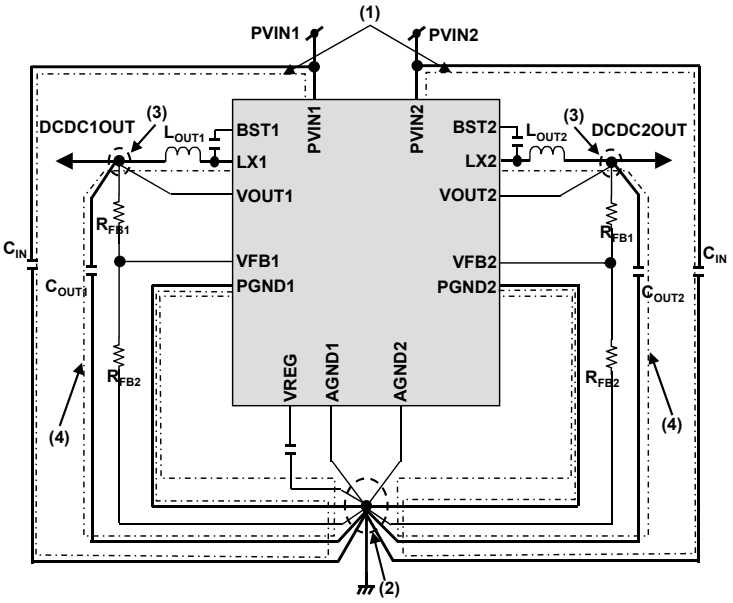

Figure A2-1 : Application circuit diagram

Note: The application circuit diagram and layout diagram explained in this section, should be used as reference examples. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit and the information attached with it, in the design of the equipment.

Established : 2014-03-19
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APPLICATIONS INFORMATION (Continued)

3. Recommended components

Reference Designator	QTY	Value	Manufacturer	Part Number	Note
CBST1, CBST2	1	0.1 µF	Murata	GRM188R72A104KA35L	—
COUT1, COUT2	4	22 µF	Murata	GRM32ER71E226KE15L	—
CPVIN1, CPVIN2	3	10 µF	TAIYO YUDEN	UMK325AB7106MM-T	—
	1	0.1 µF	Murata	GRM188R72A104KA35L	—
LOUT1, LOUT2	1	1.0 µH	Panasonic	ETQP3W1R0WFN	If V_{OUT}= 1.1 V
RFB1A, RFB2A	1	18 kΩ	Panasonic	ERJ3EKF1802V	If V_{OUT}= 1.1 V
RFB1B, RFB2B	1	0 Ω	Panasonic	ERJ3GEY0R00V	If V_{OUT}= 1.1 V
RRB1C, RFB2C	1	15 kΩ	Panasonic	ERJ3EKF1502V	If V_{OUT}= 1.1 V
RFB1D, RFB2D	1	0 Ω	Panasonic	ERJ3GEY0R00V	If V_{OUT}= 1.1 V
CVREG	1	4.7 µF	Murata	GRM21BR71A475KA73	—
CPHYIN	1	1.0 µF	Murata	GRM188R71A105KA61	—
CPHY	1	1.0 µF	Murata	GRM188R71A105KA61	—
RPG1, RPG2	1	100 kΩ	Panasonic	ERJ3EKF1003V	—
RCNTIN1	1	100 kΩ	Panasonic	ERJ3EKF1003V	Logic control for CNT1
RCNTIN2	1	100 kΩ	Panasonic	ERJ3EKF1003V	Logic control for CNT2

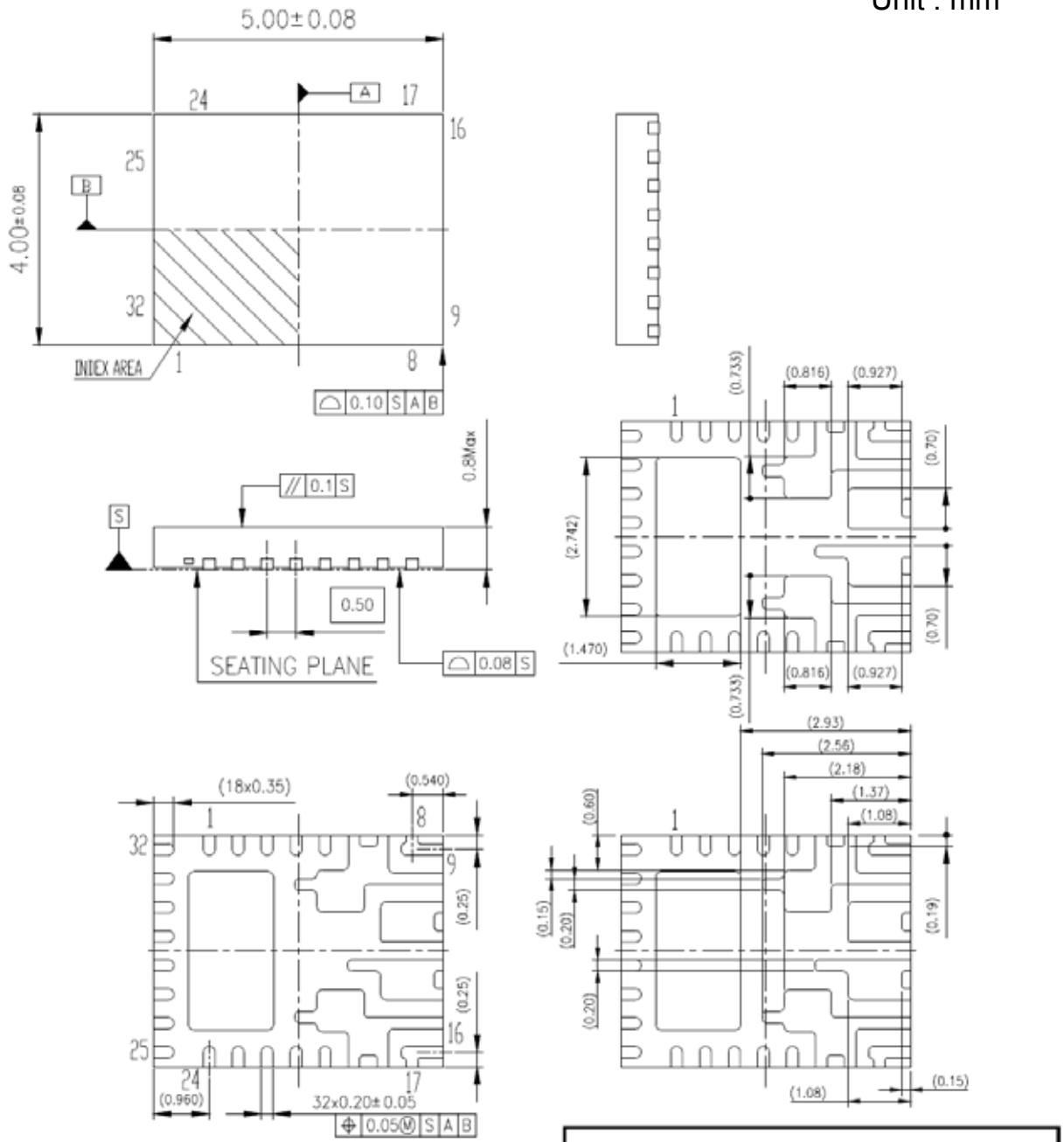
Panasonic NN30500A

PACKAGE INFORMATION

Outline Drawing

Package Code : HQFN032-A5-0405XZF

Unit : mm



Body Material : Br/Sb Free Epoxy Resin
Lead Material : Cu Alloy
Lead Finish Method : Pd Plating

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Revised : 2015-01-17

IMPORTANT NOTICE

1. When using the IC for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this IC, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. This IC is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automotive, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the IC being used for any special application, unless our company agrees to the use of such special application.
   However, for the IC which we designate as products for automotive use, it is possible to be used for automotive.
4. This IC is neither designed nor intended for use in automotive applications or environments unless the IC is designated by our company to be used in automotive applications.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the IC being used in automotive application, unless our company agrees to such application in this book.
5. Please use this IC in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our IC being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might be damaged.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
9. Take notice in the use of this IC that it might be damaged when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.
10. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
    Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the IC might be damaged before the thermal protection circuit could operate.
11. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the IC might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
12. Product which has specified ASO (Area of Safe Operation) should be operated in ASO.
13. Verify the risks which might be caused by the malfunctions of external components.
14. Connect the metallic plate (fin) on the back side of the IC to the respective potentials (AGND, PVIN1, PVIN2, LX1, LX2). The thermal resistance and electrical characteristics are guaranteed only when the metallic plate (fin) are connected with their respective potentials.

Established : 2014-03-19
Revised : 2015-01-17

Request for your special attention and precautions in using the technical information and semiconductors described in this book

(1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

(2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.

(3) The products described in this book are intended to be used for general applications (such as office equipment, communications equipment, measuring instruments and household appliances), or for specific applications as expressly stated in this book.
Consult our sales staff in advance for information on the following applications:
- Special applications (such as for airplanes, aerospace, automotive equipment, traffic signaling equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.

It is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the products described in this book for any special application, unless our company agrees to your using the products in this book for any special application.

(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

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