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RF3220

LOW NOISE, LINEAR AMPLIFIER HIGH LINEARITY/DRIVER AMPLIFIER

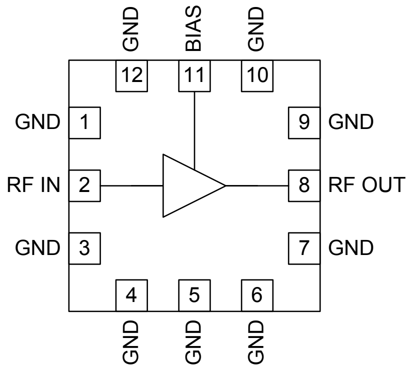
Package Style: QFN, 12-Pin, 3 x 3

Features

- 500MHz to 3GHz
- +40.8dBm Output IP3
- +14.0dB Gain at 1850MHz
- +12.5dBm Input P1dB at 1850MHz
- 2.9dB Noise Figure at 1850MHz
- Single 5V Power Supply

Applications

- Basestation Applications
- Cellular and PCS Systems
- CDMA, W-CDMA Systems
- GSM/EDGE Systems
- Final PA for Low-Power Applications



Functional Block Diagram

Product Description

The RF3220 is a high-efficiency GaAs Heterojunction Bipolar Transistor (HBT) amplifier packaged in a low-cost surface-mount package. This amplifier is ideal for use in applications requiring high-linearity and low noise figure over the 500MHz to 3GHz frequency range. The RF3220 operates from a single 5V power supply, and is assembled in an economical 3mmx3mm QFN package.

Ordering Information

RF3220	Low Noise, Linear Amplifier High Linearity/Driver Amplifier
RF3220PCBA-41X	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☑ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ RF MEMS
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
RF Input Power	+20	dBm
Device Voltage	-0.5 to +6.0	V
Device Current	200	mA
Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					V_{CC}=5V, RF_{IN}=-10dBm, Freq=1850MHz, with Temp=25°C unless otherwise noted.
AC Specifications					
Frequency		1850		MHz	
Gain	12	14.0	15.5	dB	
Output IP3	36	40		dBm	F_1= 1850MHz, F_2=1851MHz
Output P1dB	24	+25.5		dBm	
Noise Figure		2.9		dB	
Thermal					
$Theta_{JC}$		76		°C/W	
Maximum Measured Junction Temperature at DC Bias Conditions		146		°C	T_{CASE}=+85°C $I_{CC=}$ 160mA V_{CC}=5.0V
Mean Time To Failures		>100		years	T_{CASE}=+85°C
DC Specifications					
Device Voltage		5.0		V	
Operating Current Range	110	135	160	mA	

Note: The RF3220 must be operated at or below 160mA in order to achieve the thermal performance listed above.

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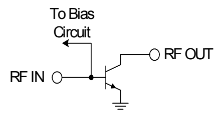
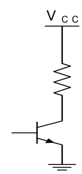
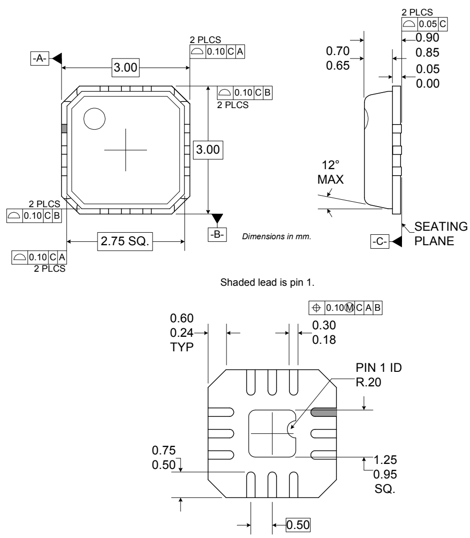
Pin	Function	Description	Interface Schematic
1	GND	Ground connection.	
2	RF IN	RF input pin. This pin is not internally DC-blocked. A DC blocking capacitor suitable for the frequency of operation should be used.	
3	GND	Ground connection.	
4	GND	Ground connection.	
5	GND	Ground connection.	
6	GND	Ground connection.	
7	GND	Ground connection.	
8	RF OUT	Amplifier output pin. This pin is an open-collector output. It must be biased to V_{CC} through a choke or matching inductor. This pin is typically matched to 50Ω with a shunt bias/matching inductor and series blocking/matching capacitor. Refer to application schematics.	See pin 2.
9	GND	Ground connection.	
10	GND	Ground connection.	
11	BIAS	This pin is used to control the bias current. An external resistor may be used to set the bias current for any V_{PD} voltage. Allows for trade-offs between IP3 versus noise figure and T_{MAX}.	
12	GND	Ground connection.	
Pkg Base	GND	Ground connection. Vias to ground required under the package base.	

Package Drawing



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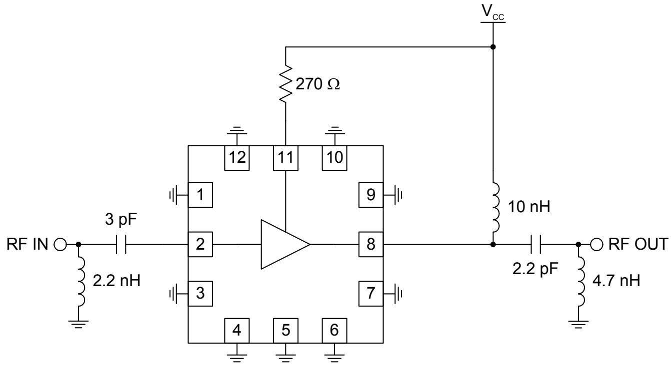
Application Schematic - 1850 MHz



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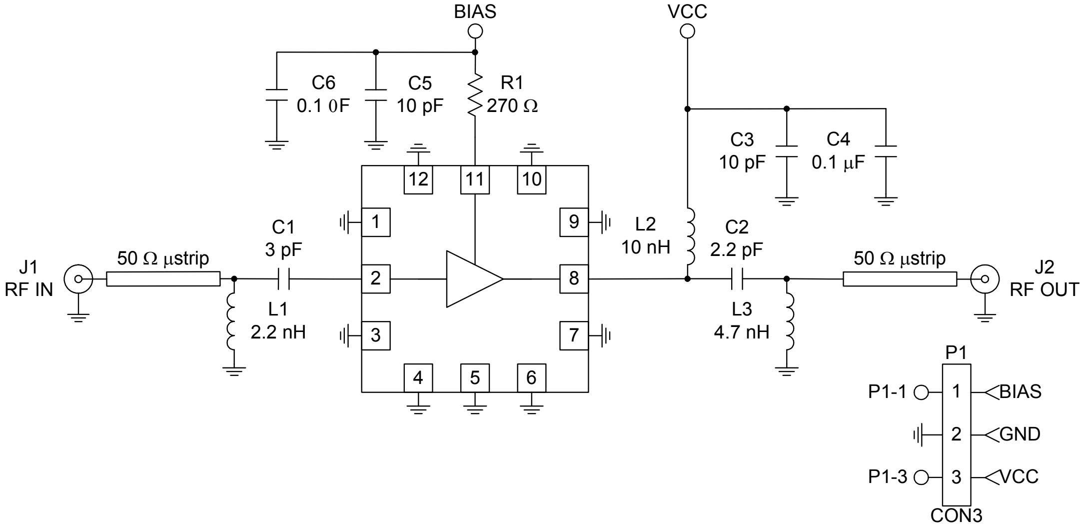
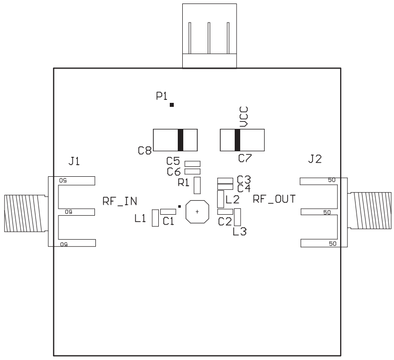
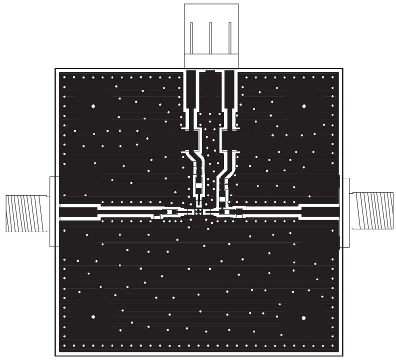
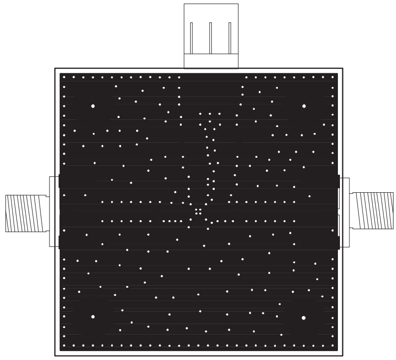
Evaluation Board Schematic



Evaluation Board Layout
Board Size 1.5" x 1.5"
Board Thickness 0.032", Board Material FR-4







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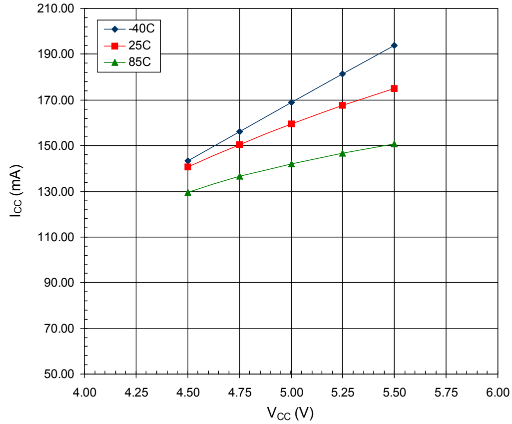
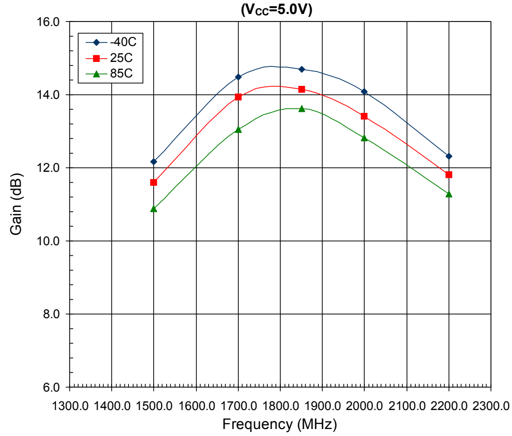
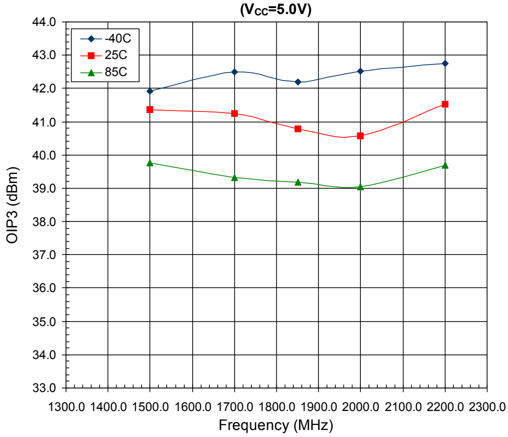
I_{CC} versus V_{CC} Across Temperature



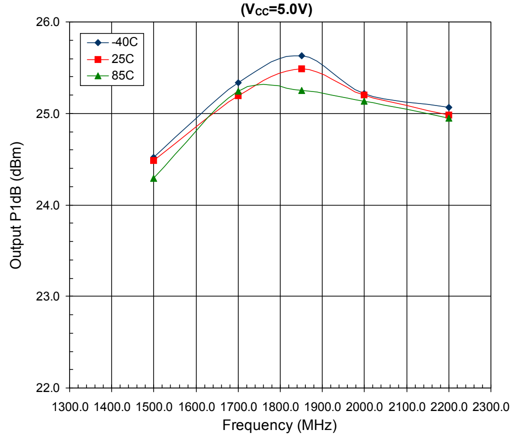
Gain versus Frequency Across Temperature
(V_{CC}=5.0V)



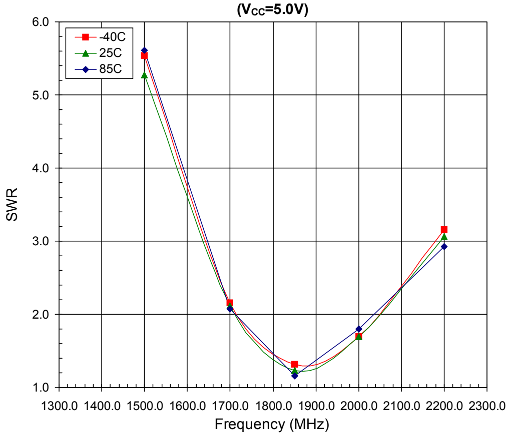
OIP3 versus Frequency Across Temperature
(V_{CC}=5.0V)



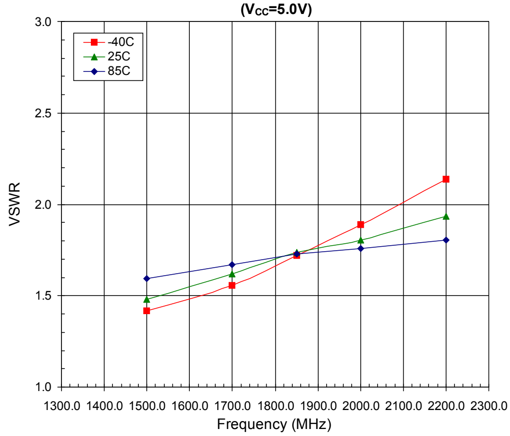
Output P1dB versus Frequency Across Temperature
(V_{CC}=5.0V)

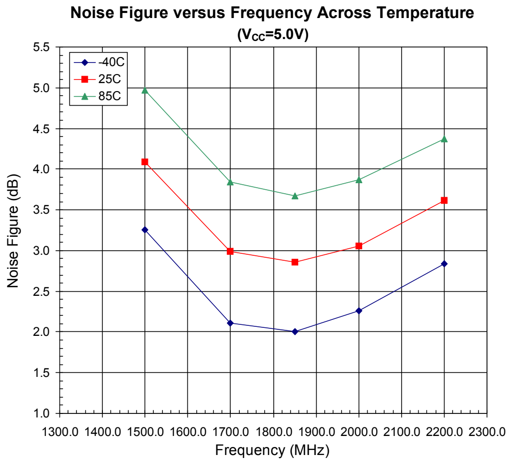


Input SWR versus Frequency Across Temperature
(V_{CC}=5.0V)



Output VSWR versus Frequency Across Temperature
(V_{CC}=5.0V)




Noise Figure versus Frequency Across Temperature
(V_{CC}=5.0V)
-40C
25C
85C
Noise Figure (dB)
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
1300.0
1400.0
1500.0
1600.0
1700.0
1800.0
1900.0
2000.0
2100.0
2200.0
2300.0
Frequency (MHz)

PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Pattern

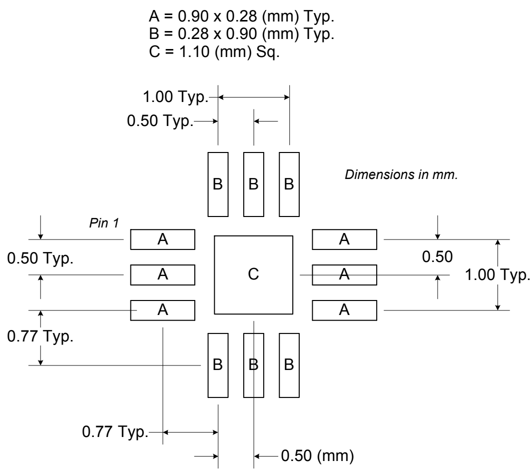


Figure 1. PCB Metal Land Pattern (Top View)

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

Thermal Pad and Via Design

The PCB metal land pattern has been designed with a thermal pad that matches the exposed die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

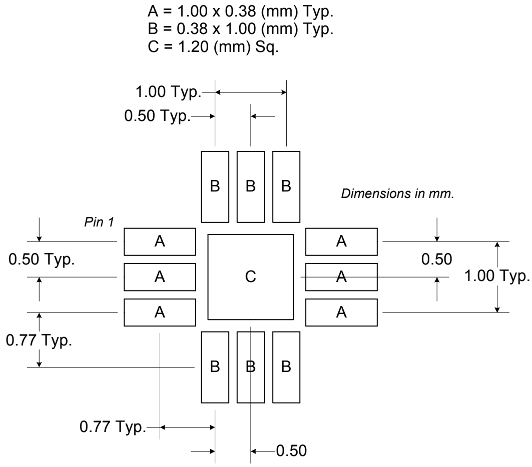


Figure 2. PCB Solder Mask Pattern (Top View)

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