Reference Manual

DOC. REV. 3/19/2009

EBX-22 (Sidewinder)

VIA Eden Based SBC with Ethernet, Video, Audio, SATA, Industrial I/O, and SPI

VERSALOGIC CORPORATION

WWW.VERSALOGIC.COM

3888 Stewart Road
Eugene, OR 97402
(541) 485-8575
Fax (541) 485-5712

Contents Copyright © 2009
All Rights Reserved

Notice:

Although every effort has been made to ensure this document is error-free, VersaLogic makes no representations or warranties with respect to this product and specifically disclaims any implied warranties of merchantability or fitness for any particular purpose.

VersaLogic reserves the right to revise this product and associated documentation at any time without obligation to notify anyone of such changes.

PC/104 and the PC/104 logo are trademarks of the PC/104 Consortium.

MEBX-22

Product Release Notes

Rev 3 Release

Production release.

Rev 2 Release

Beta release. Some functionality has not yet been implemented.

Rev 1 Release

Pre-production only. No customer releases.

Support Page

The EBX-22 support page, at **http://www.versalogic.com/private/sidewindersupport.asp**, contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- BIOS information and upgrades
- Utility routines and benchmark software

This is a private page for EBX-22 users that can be accessed only be entering this address directly. It cannot be reached from the VersaLogic homepage.

Table of Contents

1 Introduction

Description

The EBX-22 is a feature-packed single board computer designed for OEM control projects requiring fast processing, industrial I/O, flexible memory options and designed-in reliability and longevity (product lifespan). Its features include:

- VIA Eden 1.2 GHz processor
- CX700M chipset with integrated 200MHz 128-bit UniChrome Pro II 2D/3D graphics processor. Up to 128 MB unified frame buffer:
  - Microsoft DirectX 7.0, 8.0 and 9.0 compatible
  - Support OpenGL
  - MPEG-2/4 hardware decoding
  - WMV9 hardware decoding
  - Integrated HDTV/SDTV encoder
- DualView dual image capability
- Up to 1 GB system RAM
- CompactFlash and USB SSD sites
- Dual 10/100 Ethernet interface
- Flat panel display support
- DVI support through HDMI connector
- Analog video supports SVGA and YPbPr (component)
- PC/104-*Plus* expansion site
- Two SATA I channels
- IDE controller, one channel, ATA 100 compatible
- Five USB 2.0/1.1 ports
- TVS devices (on user I/O connections)
- Four COM ports (two RS-232, two RS-232/422/485)
- LPT port (floppy mode compatible)
- CPU and motherboard temperature sensors
- HD audio CODEC, one line in and one line out only
- PS/2 keyboard and mouse ports
- Industrial I/O
  - 8-channel, 12-bit analog inputs
  - 32-channel digital I/O
- SPI interface supports up to four (external) SPI devices either of user design or any of the SPX™ series of expansion boards, with clock frequencies from 1-8MHz
- Watchdog timer
- Vcc sensing reset circuit (all rails monitored, user-selectable interrupt on fault)
- EBX-compliant 5.75” x 8.00” footprint
- Field upgradeable BIOS with OEM enhancements
- ISA bus, supporting legacy I/O, memory transactions and IRQs (no DMA or bus mastering)
- Customizing available

The EBX-22 is compatible with popular operating systems such as Windows and Linux.

A full complement of standard I/O ports are included on-board. Additional I/O expansion is available through the high-speed PCI-based PC/104-*Plus* expansion site (which supports both PC/104 and PC/104-*Plus* expansion modules), and through the serial peripheral interface (SPI).

A limited ISA bus is created in the PLD to support legacy 8-bit and 16-bit PC/104 ISA cards. It supports I/O, memory, and interrupts. DMA and bus mastering are not supported.

System memory expansion is supported with one high-reliability latching 240-pin SODIMM socket. Up to 1 GB of low power, 533 MHz, PC2-4200 compatible DDR2 RAM is available.

The EBX-22 offers a wide range of video and graphics capabilities, including a 2D/3D UniChrome Pro II graphics processor, high definition MPEG-2/4 processing, high-quality video that supports RGB555/565/8888 and YUV422 video formats, as well as SVGA, flat panel display, and a TV interface that supports the YPbPr interface mode.

The EBX-22 features high reliability design and construction. It also features a watchdog timer, voltage sensing reset circuits and self-resetting fuse on the 5V supply to the keyboard, mouse, and USB.

All EBX-22 boards are subjected to functional testing and are backed by a limited two-year warranty. Careful parts sourcing and US-based technical support ensure the highest possible quality, reliability, service and product longevity for this exceptional SBC.

Technical Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Board Size: 5.75" x 8.00" x 1.75"; EBX compliant
Storage Temperature: -40° C to 85° C
Free Air Operating Temperature:
0° C to +60° C EBX-22g
Power Requirements: *(with 256 MB DDR2 SODIMM, keyboard and mouse, Windows XP)*
EBX-22g – +5.0V ± 5% @ 2.2.0A (11W) typ.
EBX-22h – TBD
+3.3V or ±12V may be required by some expansion modules
System Reset:
V_{cc} sensing, resets below 3.3V, 2.5V, or if Vcore power are not within +/- 10% of optimal values
DRAM Interface:
One 240-pin SODIMM socket
Up to 1 GB 533 MHz, PC2-4200 compatible, DDR2 RAM
Video Interface:
Analog outputs for VGA or YPbPr
Digital output, HDMI connector (DVI video only)
LVDS output for TFT FPDs
Up to 1280 x 1024 (24 bits)
2D/3D MPEG-2/4 graphics
IDE Interface:
One channel, 44-pin keyed 2mm header.
Supports up to UDMA/33.
Supports up to two IDE devices (hard drives, CD-ROM, CompactFlash, etc.)
SATA Interface:
Two SATA I headers
Ethernet Interface:
Two Intel 82551ER based fast Ethernet 10BaseT/100BaseTX controllers
Audio Interface:
HD audio codec, one Line Out and one Line In support
COM1–2 Interface:
RS-232, 16C550 compatible, 115k baud max.
COM3–4 Interface:
RS-232 4-wire, RS-422, RS-485, 16C550 compatible, 460k baud max.
LPT Interface:
Bi-directional/EPP/ECP/floppy mode compatible
Analog Input:
8-channel, 12-bit, single-ended, 500 kSPS, channel independent input range: 0 to +4.095V
Digital Interface:
32-channel, ±24 mA source and sink, 3.3V signaling
SPX Interface:
Supports 4 external SPI chips either of user design or any of the SPX™ series of expansion boards
Counter/timers:
Three PWM outputs, three TACH inputs which can be used as general purpose counter/timers
BIOS:
General Software Embedded BIOS© with OEM enhancements
Field-upgradeable with Flash BIOS Upgrade Utility
Bus Speed:
CPU Bus: 400 MHz
PC/104-*Plus* (PCI): 33 MHz
PC/104 (ISA): 8 MHz
Compatibility:
EBX – full compliance
PC/104 (ISA) – limited compliance via PCI to ISA bridge in PLD
PC/104-*Plus*) (PCI) – full compliance, 3.3V signaling, PCI 2.2 compatible
SPX™ – full compliance
Weight:
EBX-22g – 0.606 lbs (0.275 kg)
EBX-22h – TBD

Specifications are subject to change without notice.

EBX-22 Block Diagram

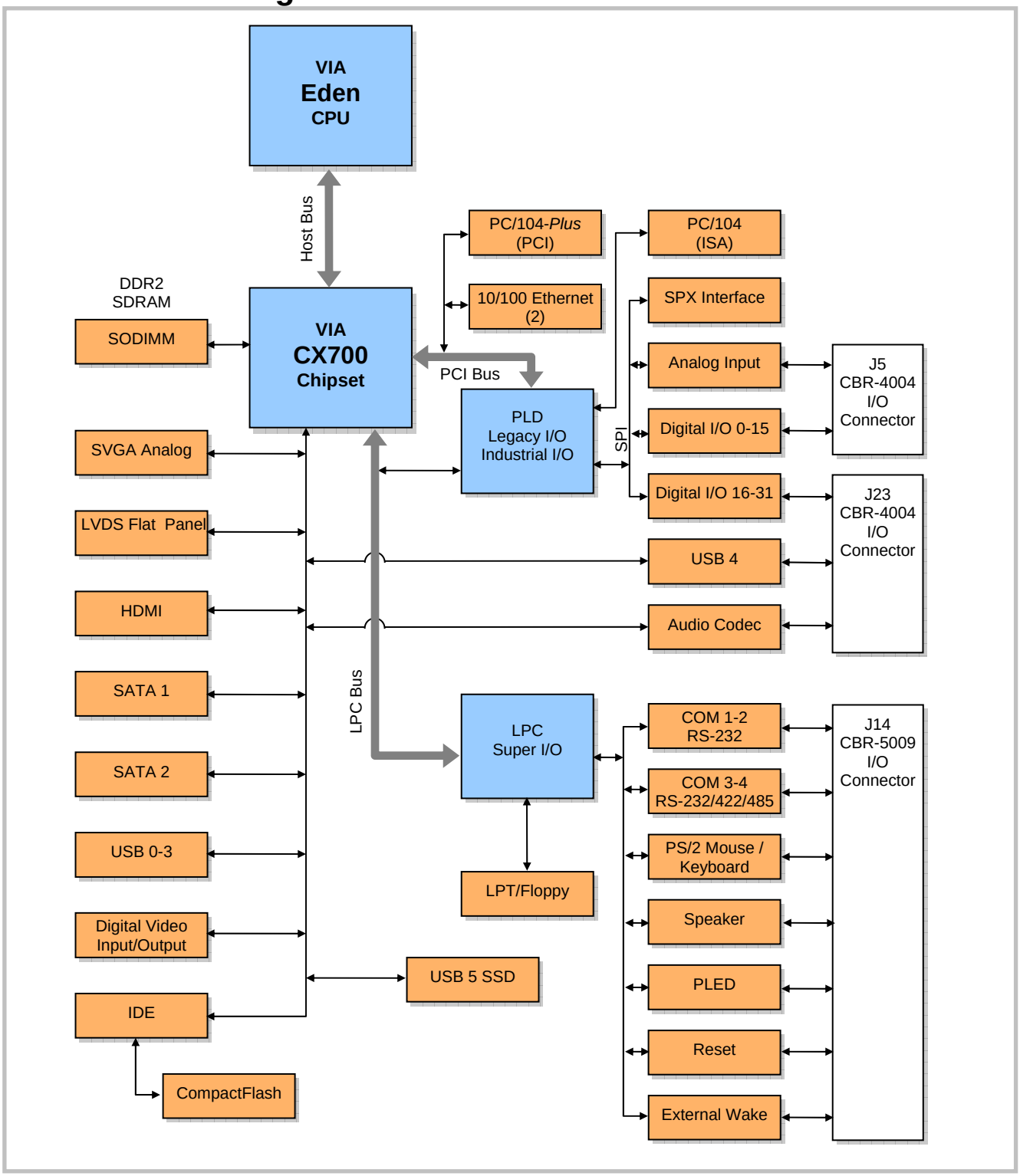


Figure 1. EBX-22 Block Diagram

CX700M Block Diagram

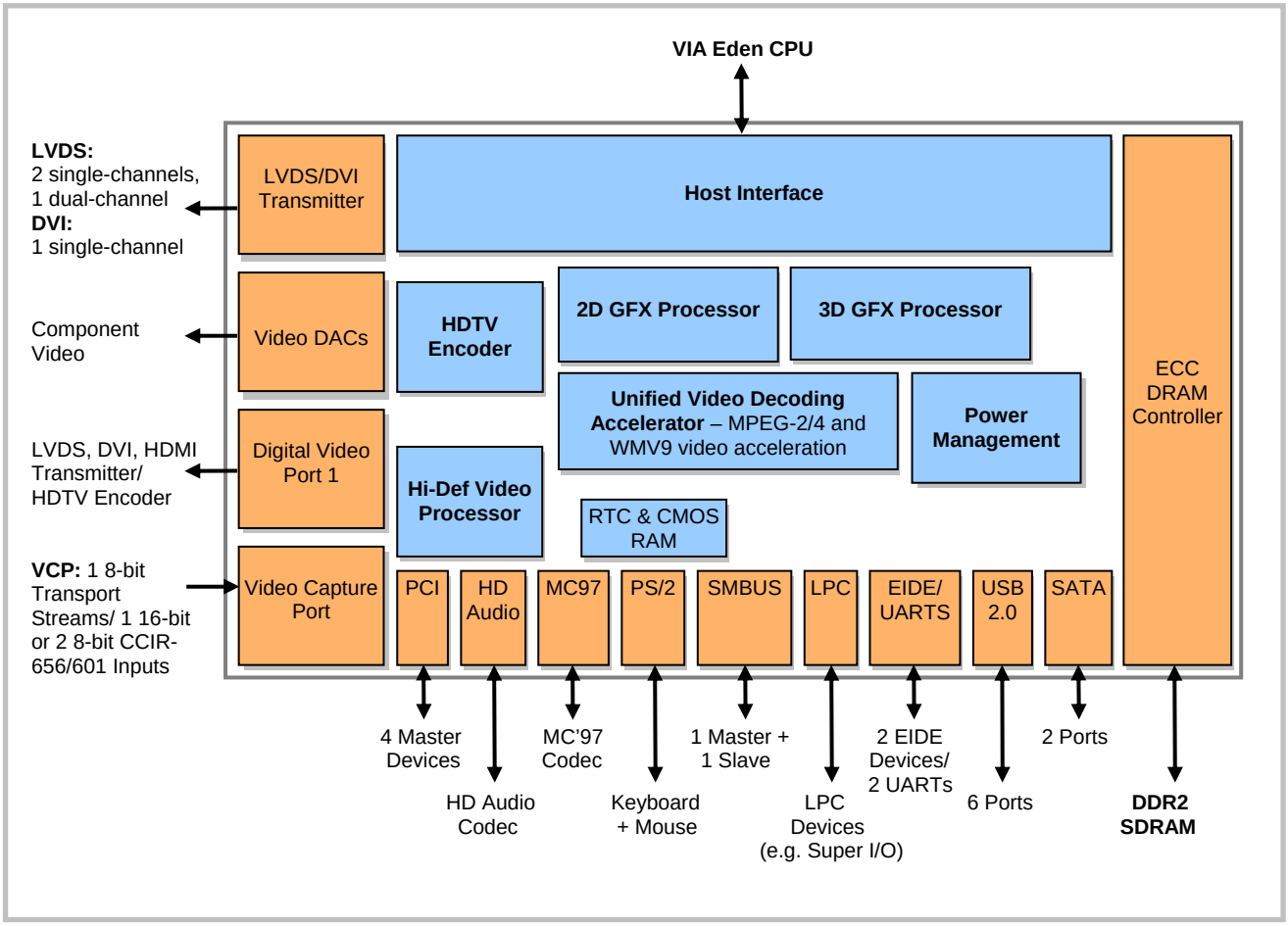


Figure 2. CX700M Block Diagram

RoHS-Compliance

The EBX-22 is RoHS-compliant.

About RoHS

In 2003, the European Union issued Directive 2002/95/EC regarding the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment.

The RoHS directive requires producers of electrical and electronic equipment to reduce to acceptable levels the presence of six environmentally sensitive substances: lead, mercury, cadmium, hexavalent chromium, and the presence of polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) flame retardants, in certain electrical and electronic products sold in the European Union (EU) beginning July 1, 2006.

VersaLogic Corporation is committed to supporting customers with high-quality products and services meeting the European Union's RoHS directive.

Warnings

ELECTROSTATIC DISCHARGE

Electrostatic discharge (ESD) can damage boards, disk drives and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

The board should also be protected inside a closed metallic anti-static envelope during shipment or storage.

Note The exterior coating on some metallic antistatic bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the bottom-side of the EBX-22.

LITHIUM BATTERY

To prevent shorting, premature failure or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of depleted batteries promptly.

MOUNTING SUPPORT

The single board computer must be supported at all eight mounting points to prevent excessive flexing when expansion modules are mated and detached. Flex damage caused by excessive force on an improperly mounted circuit board is not covered under the product warranty. See page 17 for more details.

Technical Support

If you are unable to solve a problem with this manual please visit the EBX-22 Product Support web page listed below. If you have further questions, contact VersaLogic technical support at (541) 485-8575. VersaLogic technical support engineers are also available via e-mail at Support@VersaLogic.com.

EBX-22 Support Website

http://www.versalogic.com/private/Sidewindersupport.asp

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (541) 485-8575.

Please provide the following information:

- Your name, the name of your company and your phone number
- The name of a technician or engineer that can be contact if any questions arise.
- Quantity of items being returned
- The model and serial number (barcode) of each item
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem
- The return shipping address

Warranty Repair All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair All non-warranty repairs are subject to diagnosis and labor charges, parts charges and return shipping fees. Please specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

Note Please mark the RMA number clearly on the outside of the box before returning. Failure to do so can delay the processing of your return.

Configuration and Setup 2

Initial Configuration

The following components are recommended for a typical development system. Note that this is a recommended configuration only.

Note You may substitute other components for the ones listed below, such as a PS/2 mouse and keyboard, a parallel ATA hard drive or CD-ROM drive, or another type of monitor. If you substitute other components, be sure to adjust the basic setup steps accordingly.

- EBX-22 single board computer
- 240-pin SODIMM (memory module): DDR2-400 or DDR2-533
- ATX power supply with motherboard and drive connectors
- SVGA video monitor
- USB keyboard and mouse
- SATA hard drive
- USB CD-ROM drive

The following VersaLogic cables are recommended.

- Video adapter cable (CBR-1201)
- SATA data cable (CBR-0701)
- ATX to SATA power adapter cable (CBR-0401)
- Power adapter cable (CBR-2022)

You will also need a Windows (or other OS) installation CD.

Basic Setup

The following steps outline the procedure for setting up a typical development system. The EBX-22 should be handled at an ESD workstation or while wearing a grounded antistatic wrist strap.

Before you begin, unpack the EBX-22 and accessories. Verify that you received all the items you ordered. Inspect the system visually for any damage that may have occurred in shipping. Contact Support@VersaLogic.com immediately if any items are damaged or missing.

Gather all the peripheral devices you plan to attach to the EBX-22 and their interface and power cables.

It is recommended that you attach standoffs to the board (see Hardware Assembly) to stabilize the board and make it easier to work with.

Figure 3 shows a typical start-up configuration.

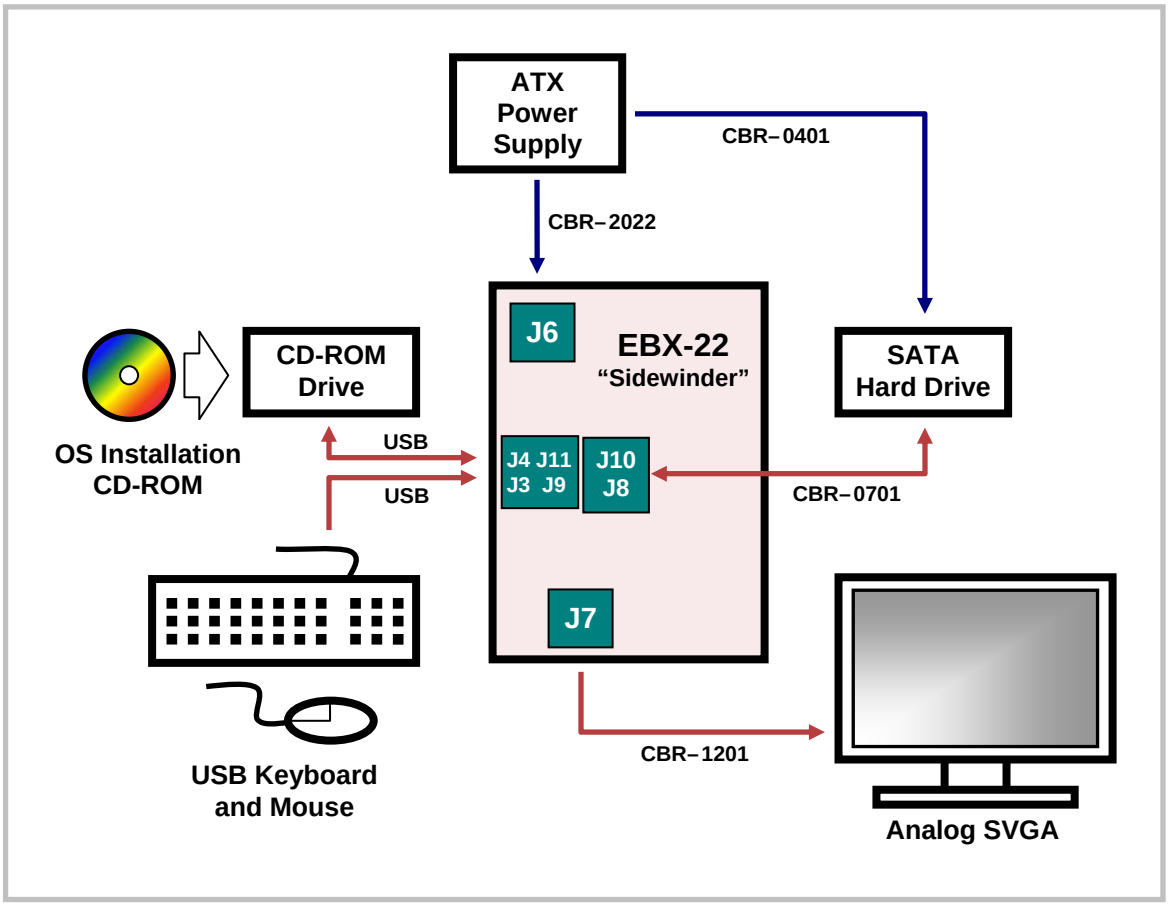


Figure 3. Typical Start-up Configuration

1. Install Memory

- Insert the DDR2 DRAM module into the SODIMM socket J2 and latch it into place.

2. Attach Cables and Peripherals

- Plug the video adapter cable CBR-1201 into socket J7. Attach the video monitor interface cable to the video adapter.
- Plug the USB CD-ROM drive, keyboard, and mouse into on-board USB sockets (J3, J4, J9, or J11).
- Plug the SATA data cable CBR-0701 into socket J8 or J10, and attach the SATA hard drive to the cable.

Note The mating connector on some SATA data cables may interfere with the proper seating of a PC/104-*Plus* (PCI) expansion board at connector J17. The SATA specification does not specify exterior dimensions for connector housings, and some manufacturers make wider housings than others. The 3M 5602 Series straight SATA connector is 0.22 in. wide and will interfere less with the PC/104-*Plus* card. Even with thinner SATA cables, you may need to ease the cable(s) away from the PC/104-*Plus* connector to seat the expansion board completely.

- Attach an ATX power cable to the SATA hard drive.

3. Attach Power

- Plug the power adapter cable CBR-2022 into connector J6. Attach the motherboard connector of the ATX power supply to the adapter.

4. Soft Power Button Configuration

- The EBX-22 requires activation of the soft power button to power up. This can be executed manually or automatically. Installing a jumper on pins V5[1-2] causes the EBX-22 to create its own soft power pulse automatically when power is applied. If a jumper is installed at V5[3-4], you will have to create a pulse on pin 40 of I/O connector J14. This can be done by shorting pin 40 to ground for 100 to 500 ms.

5. Review Configuration

- Before you power up the system, double check all the connections. Make sure all cables are oriented correctly and that adequate power will be supplied to the EBX-22 and peripheral devices.
- Verify that jumper V1[1-2] is installed. This connects the battery to the 32 kHz clock and CMOS. The board will not turn on with out this connection.

6. Power On

- Turn on the ATX power supply and the video monitor. If the system is correctly configured, a video signal should be present.

7. Select a Boot Drive

- During startup, press the B key to display the boot menu. Insert the OS installation CD in the CD-ROM drive, and select to boot from the CD-ROM drive.

8. Install Operating System

- Install the operating system according to the instructions provided by the OS manufacturer. (See Operating System Installation.)

Note If you intend to operate the EBX-22 under Windows XP or Windows XP Embedded, be sure to use Service Pack 2 (SP2) and all updates for full support of the latest hardware features.

CMOS Setup

The default CMOS Setup parameters for the EBX-22 are shown below. Due to changes and improvements in the system BIOS, the information on your monitor may differ from that shown below. The factory default date will correspond to the BIOS build date. Some values may vary depending on the configuration of your EBX-22.

Main Tab

```
  Main    Exit    Boot    POST    SIO    Features    Firmbase    Misc    Board
+ ---------------------------------------------------- + ------------------- +
|                                                      |                     |
| System Summary                                       |Use TAB to switch    |
| ---------------------------------------------------- |between month, day   |
| General Software[R] System BIOS                      |and year.  Use digits|
| BIOS Core Version     EB(SF).003                     |and BKSP to change   |
| VersaLogic Version    6.3.102                        |field.               |
| BIOS Build Date       03/19/08                       |                     |
| System BIOS Size      128KB                          |                     |
| CPM/CSPM/BPM Modules  P7C7, CX700, EBX22             |                     |
| StrongFrame[TM] Technology, Firmbase[R] Technology   |                     |
|                                                      |                     |
| Processor (CPU)                                      |                     |
| VIA Eden Processor 1200MHz                           |                     |
|                                                      |                     |
| System Memory (RAM)                                  |                     |
| Low Memory (KB)       627                            |                     |
| Extended Memory (KB)  449344                         |                     |
|                                                      |                     |
| Real Time Clock (RTC)                                |                     |
| RTC Date              [03/26/2008]                   |                     |
| RTC Time              [13:57:20]                     |                     |
+ ---------------------------------------------------- + ------------------- +
```

Exit Tab

```
  Main    Exit    Boot    POST    SIO    Features    Firmbase    Misc    Board
+ ---------------------------------------------------- + ------------------- +
| Save, Restore, and Exit Setup                        |Press ENTER to save  |
| ---------------------------------------------------- |changes and reboot   |
| Save Settings and Restart             [Enter]        |system.              |
|                                                      |                     |
| Exit Setup Without Saving Changes     [Enter]        |                     |
|                                                      |                     |
| Reload Factory-Defaults and Restart   [Enter]        |                     |
|                                                      |                     |
| Reload Custom-Defaults and Restart    [Enter]        |                     |
+ ---------------------------------------------------- + ------------------- +
```

Boot Tab

```
  Main    Exit    Boot    POST    SIO    Features    Firmbase    Misc    Board
+ ------------------------------------------------------ + ------------------ +
| System Boot Configuration                              |Select initialization|
| ------------------------------------------------------ |and boot priority for|
|                                                        |all devices.         |
| Boot Device Prioritization (BBS)                       |                     |
| 0 [IDE 2/ATA Master]                                   |Backspace deletes    |
| 1 [None]                                               |selection.  Space    |
|                                                        |bar, + and - change  |
| Initialization Policy [All Devices]                    |selections.          |
|                                                        |                     |
| Floppy Drive Configuration                             |                     |
| Floppy 0      [1.44 MB, 3.5]                           |                     |
|                                                        |                     |
| IDE Drive Configuration                                |                     |
| IDE 0 Type    [Autoconfig]                             |                     |
| IDE 0 Mode    [UDMA mode (80-conductor cable)]         |                     |
| IDE 1 Type    [Autoconfig]                             |                     |
| IDE 1 Mode    [UDMA mode (80-conductor cable)]         |                     |
| IDE 2 Type    [Autoconfig]                             |                     |
| IDE 2 Mode    [UDMA mode (40-conductor cable)]         |                     |
| IDE 3 Type    [Autoconfig]                             |                     |
| IDE 3 Mode    [UDMA mode (40-conductor cable)]         |                     |
|                                                        |                     |
| VT8237 ATA Controller Configuration                    |                     |
| ------------------------------------------------------ |                     |
| PATA Controller              [Compatible Mode]         |                     |
| SATA Controller              [Native Mode]             |                     |
+ ------------------------------------------------------ + ------------------ +
```

POST Tab

```
  Main    Exit    Boot    POST    SIO    Features    Firmbase    Misc    Board
+ ------------------------------------------------------ + ------------------ +
| POST Memory Tests                                      |Enable basic memory  |
| ------------------------------------------------------ |confidence test below|
| Low Memory Standard Test     [Disabled]                |1MB during POST.     |
| Low Memory Exhaustive Test   [Disabled]                |                     |
| High Memory Standard Test    [Disabled]                |                     |
| High Memory Exhaustive Test  [Disabled]                |                     |
| Click During Memory Test     [Disabled]                |                     |
| Clear Memory During Test     [Disabled]                |                     |
|                                                        |                     |
| POST Error Control                                     |                     |
| ------------------------------------------------------ |                     |
|                                                        |                     |
| POST User Interface                                    |                     |
| ------------------------------------------------------ |                     |
| POST Display Messages        [Enabled]                 |                     |
| POST Operator Prompt         [Enabled]                 |                     |
| POST Display PCI Devices     [Enabled]                 |                     |
|                                                        |                     |
| POST Debugging                                         |                     |
| ------------------------------------------------------ |                     |
| Post Slow Reboot Cycle       [Disabled]                |                     |
| POST Fast Reboot Cycle       [Disabled]                |                     |
|                                                        |                     |
| Device Initialization                                  |                     |
| ------------------------------------------------------ |                     |
| POST Floppy Seek             [Disabled]                |                     |
| POST Hard Disk Seek          [Enabled]                 |                     |
+ ------------------------------------------------------ + ------------------ +
```

SIO Tab

```
  Main    Exit    Boot    POST    SIO    Features    Firmbase    Misc    Board
+ ------------------------------------------------- + ------------------ +
| BIOS Super I/O Configuration                      |                    |
| ------------------------------------------------- |                    |
|                                                   |                    |
| SCH3114 Devices                                   |                    |
| ------------------------------------------------- |                    |
| Parallel Port (J29)          [Enabled]            |                    |
|   Address                    [378h]               |                    |
|   IRQ                        [IRQ 7]              |                    |
|   DMA                        [Channel 4]          |                    |
|   Mode                       [Printer]            |                    |
| Serial Port 1 (J3 Top)       [Enabled]            |                    |
|   Address                    [3f8h]               |                    |
|   IRQ                        [IRQ 4]              |                    |
| Serial Port 2 (J3 Bot)       [Enabled]            |                    |
|   Address                    [2f8h]               |                    |
|   IRQ                        [IRQ 3]              |                    |
| Serial Port 3 (J6)           [Disabled]           |                    |
|   Address                    [3e8h]               |                    |
|   IRQ                        [No IRQ]             |                    |
|   Mode                       [RS-232 (4-wire)]    |                    |
| Serial Port 4 (J5)           [Disabled]           |                    |
|   Address                    [2e8h]               |                    |
|   IRQ                        [No IRQ]             |                    |
|   Mode                       [RS-232 (4-wire)]    |                    |
+ ------------------------------------------------- + ------------------ +
```

Features Tab

```
  Main    Exit    Boot    POST    SIO    Features    Firmbase    Misc    Board
+ ------------------------------------------------- + ------------------ +
| BIOS Feature Configuration                        |Enable to initialize |
| ------------------------------------------------- |APICs and use them in|
| Interrupt Processing         [Use APIC]           |an emulated PIC mode.|
| Quick Boot                   [Enabled]            |If you wish to use   |
| Advanced Power Management    [Disabled]           |full-APIC mode, this |
| ACPI                         [Enabled]            |must be set AND      |
| POST Memory Manager          [Disabled]           |either ACPI or MP    |
| System Management BIOS       [Enabled]            |must be enabled. DO  |
| Manufacturing Mode           [Disabled]           |NOT CHANGE AFTER OS  |
| Splash Screen                [Disabled]           |INSTALL.             |
|                                                   |                     |
| Console Redirection                               |                     |
| ------------------------------------------------- |                     |
| Use Console Assignments Below [On Remote User Detect]                    |
| POST Console                 [COM1]               |                     |
| Preboot Console              [COM1]               |                     |
| Debugger Console             [COM1]               |                     |
|                                                   |                     |
| CPU Configuration                                 |                     |
| ------------------------------------------------- |                     |
| CPU Speed                    [1200 MHz]           |                     |
| Microcode Update             [Enabled]            |                     |
+ ------------------------------------------------- + ------------------ +
```

Firmbase Tab

```
  Main    Exit    Boot    POST    SIO    Features    Firmbase    Misc    Board
+ ------------------------------------------------------ + ------------------- +
| Features Enabled by Firmbase[R] Technology             |Enable to support USB|
| ------------------------------------------------------ |keyboard and mouse   |
| Legacy USB                    [Enabled]                |                     |
| USB Boot                      [Enabled]                |                     |
| EHCI/USB 2.0                  [Enabled]                |                     |
| Firmbase Disk I/O             [Disabled]               |                     |
|                                                        |                     |
| Basic Firmbase[R] Technology Configuration             |                     |
| ------------------------------------------------------ |                     |
| Firmbase Technology           [Enabled]                |                     |
| Firmbase Debug Log            [None]                   |                     |
| Firmbase System Console       [None]                   |                     |
| Firmbase Shell on Serial Port [None]                   |                     |
| Quiet Mode                    [Disabled]               |                     |
| Strict Mode                   [Enabled]                |                     |
| Bypass Mode                   [Enabled]                |                     |
| TCB Security                  [Enabled]                |                     |
| Statistics                    [Enabled]                |                     |
| Clear Memory                  [Disabled]               |                     |
| Use TSC                       [Enabled]                |                     |
| Timer Optimization            [Disabled]               |                     |
| Debug Yields                  [Disabled]               |                     |
|                                                        |                     |
| ...                                                    |                     |
|                                                        |                     |
+ ------------------------------------------------------ + -------------------+
```

Note: It is strongly advised that settings on this tab beyond the Basic Firmbase Technology Configuration section not be changed.

Misc Tab

```
+ ------------------------------------------------------ + ------------------- +
| Cache Control                                          |Enable to allow CPU  |
| ------------------------------------------------------ |level cache to       |
| CPU Cache                     [Enabled]                |operate.             |
| System Cache                  [Enabled]                |                     |
|                                                        |                     |
| Keyboard Control                                       |                     |
| ------------------------------------------------------ |                     |
| Keyboard Numlock LED          [Disabled]               |                     |
| Typematic Rate                [30/sec]                 |                     |
| Typematic Delay               [250ms]                  |                     |
|                                                        |                     |
| Miscellaneous BIOS Configuration                       |                     |
| ------------------------------------------------------ |                     |
| Lowercase Hex Displays        [Disabled]               |                     |
|                                                        |                     |
|                                                        |                     |
|                                                        |                     |
+ ------------------------------------------------------ + ------------------- +
```

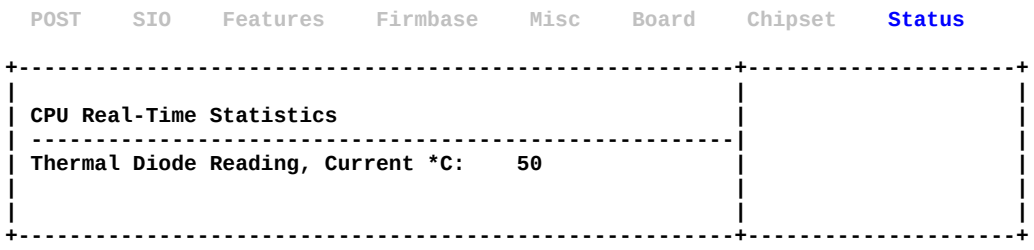
Board Tab

```
  Main    Exit    Boot    POST    SIO    Features    Firmbase    Misc    Board
+ ------------------------------------------------------ + ------------------- +
| Flash Protection              [Enabled]                 |Write-protect Flash  |
|                                                         |BIOS sectors.        |
| PCI Interrupt Configuration                             |                     |
| ------------------------------------------------------- |                     |
| PCI INT A routing             [IRQ 11]                  |                     |
| PCI INT B routing             [IRQ 11]                  |                     |
| PCI INT C routing             [IRQ 11]                  |                     |
| PCI INT D routing             [IRQ 9]                   |                     |
|                                                         |                     |
| ISA Interrupt Configuration                             |                     |
| ------------------------------------------------------- |                     |
| ISA IRQ 3                     [Disabled]                |                     |
| ISA IRQ 4                     [Disabled]                |                     |
| ISA IRQ 5                     [Disabled]                |                     |
| ISA IRQ 10                    [Disabled]                |                     |
|                                                         |                     |
| Hardware Monitoring Interrupt Configuration             |                     |
| ------------------------------------------------------- |                     |
| Voltage IRQ enable            [Disabled]                |                     |
| Overtemp IRQ enable           [Disabled]                |                     |
| CPU overtemp threshold, *C    [95]                      |                     |
| Board overtemp threshold, *C  [60]                      |                     |
| Voltage or Temperature IRQ    [None]                    |                     |
|                                                         |                     |
|                                                         |                     |
+ ------------------------------------------------------ + ------------------- +
```

Chipset Tab

```
  Boot    POST    SIO    Features    Firmbase    Misc    Board    Chipset
+ ------------------------------------------------------ + ------------------- +
|                                                         |Select video output  |
| Display Device Configuration                            |device.              |
| ------------------------------------------------------- |Some modes may       |
| Video Output Device           [VGA]                     |require a different  |
| LCD Device Type               [1]                       |Video BIOS support.  |
| Expansion/Centering           [Expansion]               |                     |
| DVI Connector                 [Present]                 |                     |
| TV Output Connector           [Component 0 (YPbPr)]     |                     |
| TV Output Format              [NTSC]                    |                     |
|                                                         |                     |
| Memory Configuration                                    |                     |
| ------------------------------------------------------- |                     |
| DQS Input Delay Control       [Auto]                    |                     |
| DQS Input Delay               [13]                      |                     |
|                                                         |                     |
| CX700 Chipset Feature Configuration                     |                     |
| ------------------------------------------------------- |                     |
| Video Frame Buffer Size       [64 MB]                   |                     |
| AGP Aperture Size             [128 MB]                  |                     |
|                                                         |                     |
|                                                         |                     |
+ ------------------------------------------------------ + ------------------- +
```

Status Tab



Operating System Installation

The standard PC architecture used on the EBX-22 makes the installation and use of most of the standard x86 processor-based operating systems very simple. The operating systems listed on the VersaLogic OS Compatibility Chart use the standard installation procedures provided by the maker of the OS. Special optimized hardware drivers for a particular operating system, or a link to the drivers, are available at the EBX-22 Product Support web page at **http://www.versalogic.com/private/Sidewindersupport.asp.**

Note An operating system installed on a different type of computer is not guaranteed to work on the EBX-22. This is referred to as a "foreign" installation. A hard disk that was used to boot a different computer cannot necessarily be moved to the EBX-22 and expected to boot. Even when porting an OS image from one revision of the EBX-22 to another, performance might fail or be impaired. For the best results, perform a fresh installation of the OS on each system. This restriction does not apply if you are producing multiple identical systems.

Dimensions and Mounting

The EBX-22 complies with all EBX standards which provide for specific mounting hole and PC/104-*Plus* stack locations as shown in the diagram below.

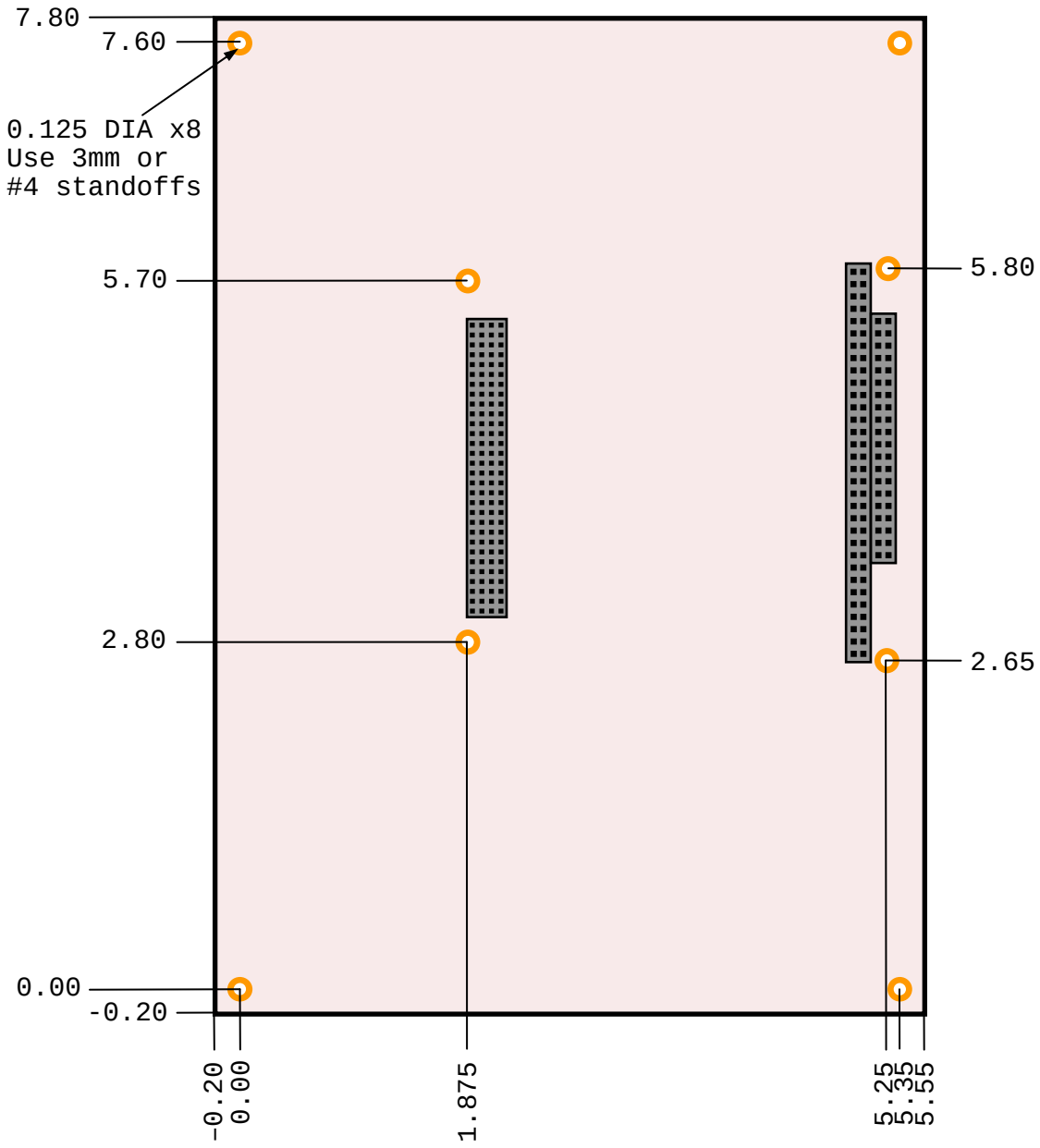


Figure 4. EBX-22 Dimensions and Mounting Holes
(Not to scale. All dimensions in inches.)

Caution The EBX-22 must be supported at all eight mounting points to prevent excessive flexing when expansion modules are mated and demated. Flex damage caused by excessive force on an improperly mounted circuit board is not covered under the product warranty.

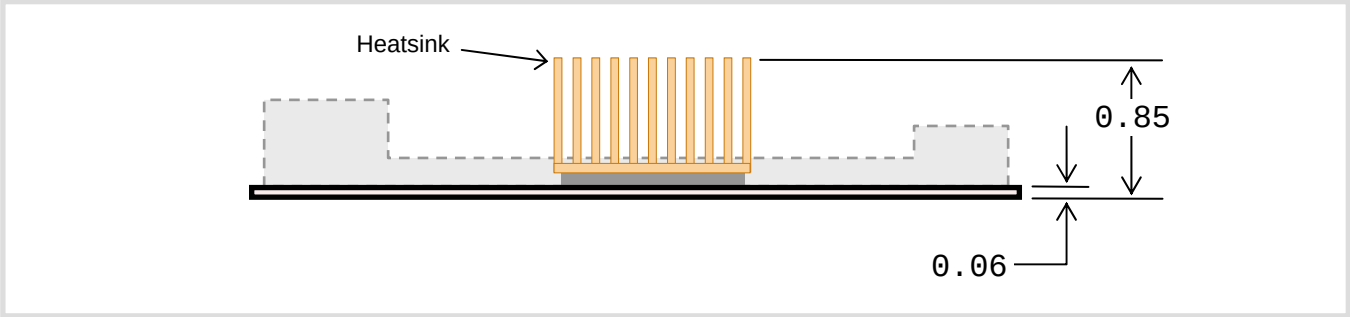


Figure 5. EBX-22 Height Dimensions
(Not to scale. All dimensions in inches.)

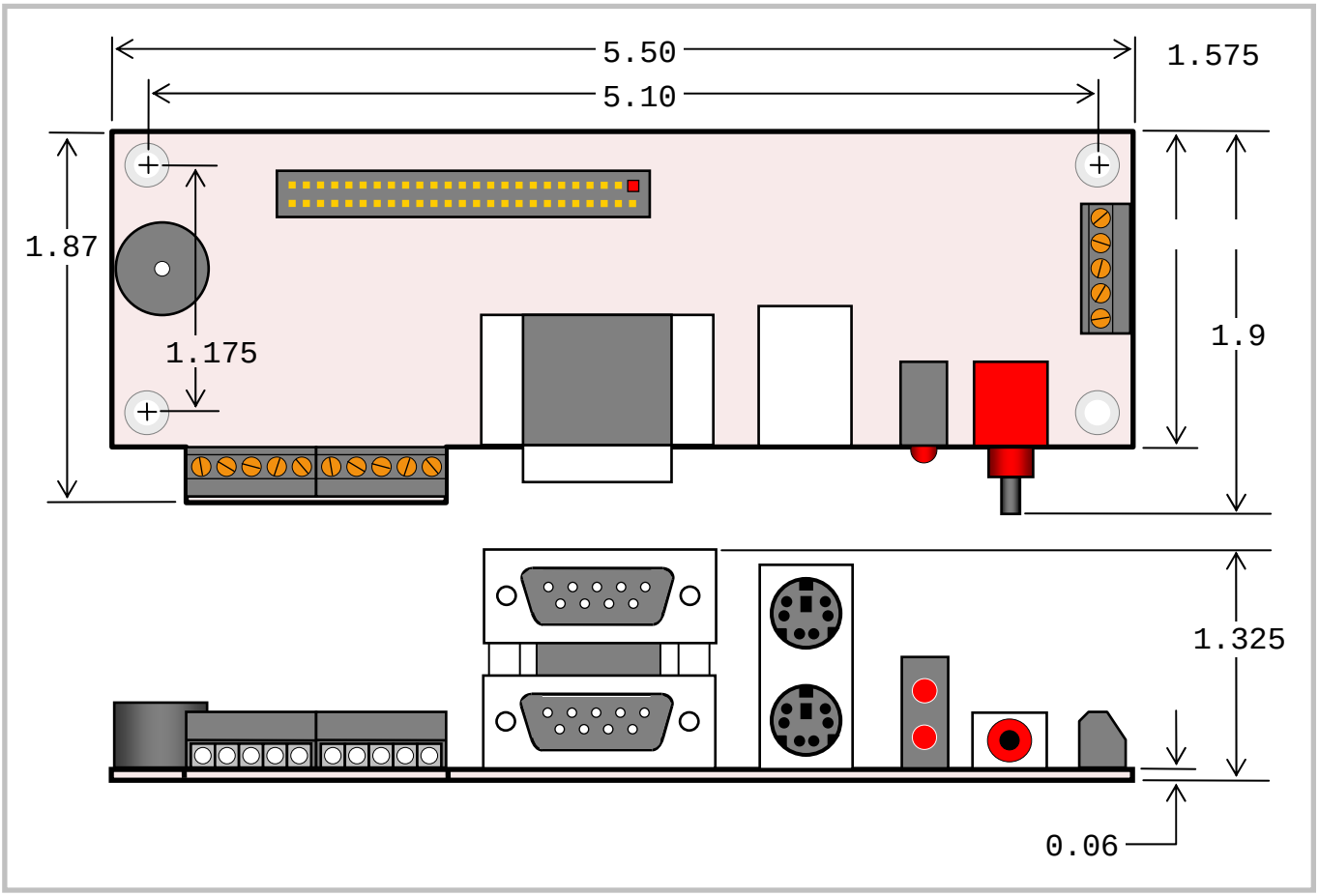


Figure 6. CBR-5009 Dimensions and Mounting Holes
(Not to scale. All dimensions in inches.)

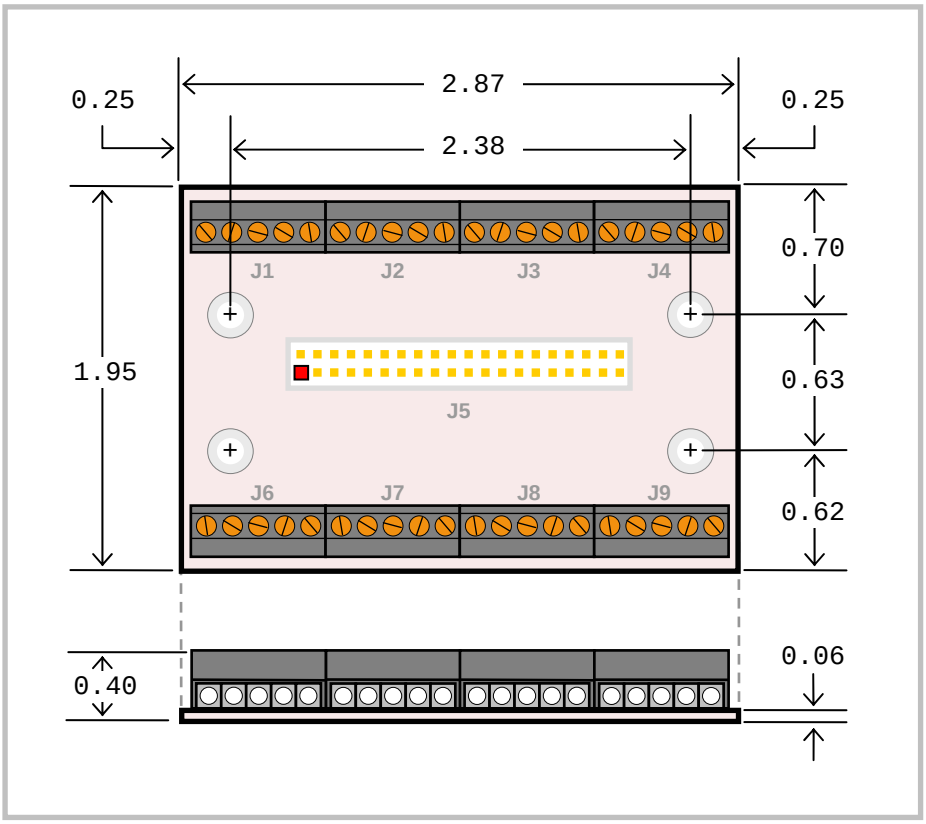


Figure 7. CBR-4004 Dimensions and Mounting Holes
(Not to scale. All dimensions in inches.)

HARDWARE ASSEMBLY

The EBX-22 mounts on four hardware standoffs using the corner mounting holes (A). These standoffs are secured to the underside of the circuit board using pan head screws.

Four additional standoffs (B) must be used under the circuit board to prevent excessive flexing when expansion modules are mated and separated. These are secured with four male-female standoffs (C), threaded from the top side, which also serve as mounting struts for the PC/104 stack.

The entire assembly can sit on a table top or be secured to a base plate. When bolting the unit down, make sure to secure all eight standoffs (A and B) to the mounting surface to prevent circuit board flexing.

An extractor tool is available (part number VL-HDW-201) to separate the PC/104 modules from the stack.

Note Standoffs and screws are available as part number VL-HDW-101.

STANDOFF LOCATIONS

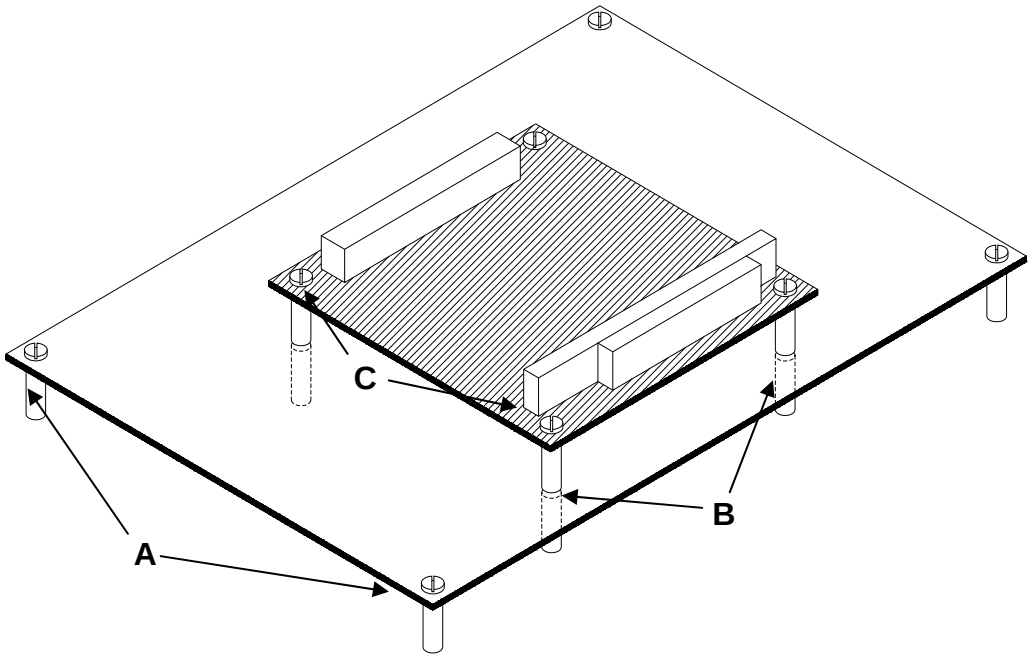


Figure 8. Standoff Locations

External Connectors

EBX-22 Connectors

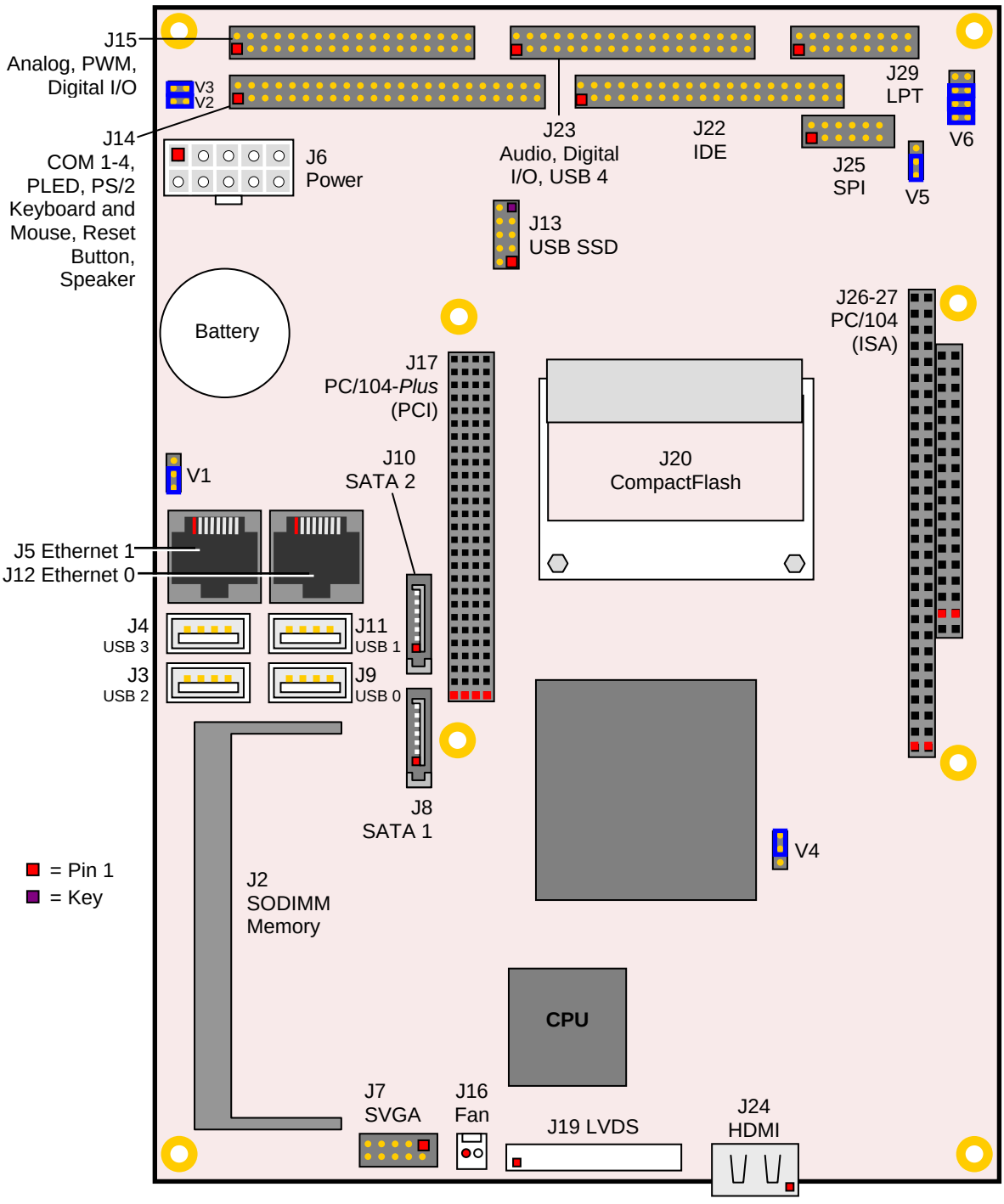


Figure 9. EBX-22 Connectors

EBX-22 CONNECTOR FUNCTIONS AND INTERFACE CABLES

The following table notes the function of each connector, as well as mating connectors and cables, and the page where a detailed pinout or further information is available.

Table 1: Connector Functions and Interface Cables

Connector[1]	Function	Mating Connector	Cable	Cable Description	Page
J2	Memory	DDR2 DRAM	–	–	29
J3	USB 2	USB Series A Plug	–	–	40
J4	USB 3	USB Series A Plug	–	–	40
J5	Ethernet 1	RJ45 Crimp-on Plug	–	–	47
J6	Main Power Input (EBX Compliant)	Molex 39-01-2100 Molex 39-00-0059 (10 ea.)	CBR-2022	6" ATX to EPIC power cable	27
J7	SVGA Video Output	FCI 89361-712LF or FCI 89947-712LF	CBR-1201	1' 12-pin 2mm IDC to 15-pin HD D-Sub VGA	43
J8	SATA 1	Standard SATA	CBR-0701; CBR-0401	500mm (19.75") 7-pin, straight-to-straight SATA data; ATX to SATA power adapter	35
J9	USB 0	USB Series A Plug	–	–	40
J10	SATA 2	Standard SATA	CBR-0701; CBR-0401	500mm 7-pin, straight to straight SATA data; ATX to SATA power adapter	35
J11	USB 1	USB Series A Plug	–	–	40
J12	Ethernet 0	RJ45 Crimp-on Plug	–	–	47
J13	USB Solid State Drive	Intel Z-U130 SSD, 2mm socket	–	–	40
J14	COM 1-4, PLED, PS/2 Keyboard and Mouse, Reset Button, Speaker, External Wake	FCI 89361-350LF	CBR-5009A	18" 2mm 50-pin to 50-pin IDC to breakout board CBR-5009B	31
J15	Digital I/O 0-15, A/D 0-7, Reset, PLD, PWM 1-3	FCI 89361-340LF	CBR-4004A	12" 2mm 40-pin to 40-pin IDC to CBR-4004B board	32
J16	CPU Fan	–	–	Fan power cable with 2-pin connector	–
J17	PC-104-*Plus*	AMP 1375799-1	–	–	69
J19	LVDS	20-pin, PanelMate 1.25mm	CBR-2010 or CBR-2011	18-bit TFT FPD using 20-pin Hirose 18-bit TFT FPD using 20-pin JAE	44
J20	CompactFlash	Type I or Type II Compact Flash	–	–	40
J22	IDE Hard Drive	FCI 89947-144LF	CBR-4406 CBR-4405[2]	18" 2mm IDE cable 2mm to 0.1" adapter	34
J23	USB 4, Digital I/O 16-31, Audio	FCI 89361-340LF	CBR-4004A	12" 2mm 40-pin to 40-pin IDC to CBR-4004B board	40
J24	HDMI	Standard HDMI	–	19-pin HDMI, video only	45
J25	SPI	FCI 89361714LF	CBR-1401 or CBR-1402	2mm 14-pin IDC, 2 or 4 SPX device cable	
J26, J27	PC/104	AMP 1375795-2	–	–	69
J29	LPT/Floppy	FCI 89361720LF	CBR-2003	12" 2mm 20-pin IDC LPT	38

1. Connectors J1 and J28 are for factory use only. Connectors J18 and J21 are not installed.
2. CBR-4405 44-pin to 40-pin adapter is required to connect to 3.5-inch IDE drives with 40-pin connectors.

CBR-5009 CONNECTORS

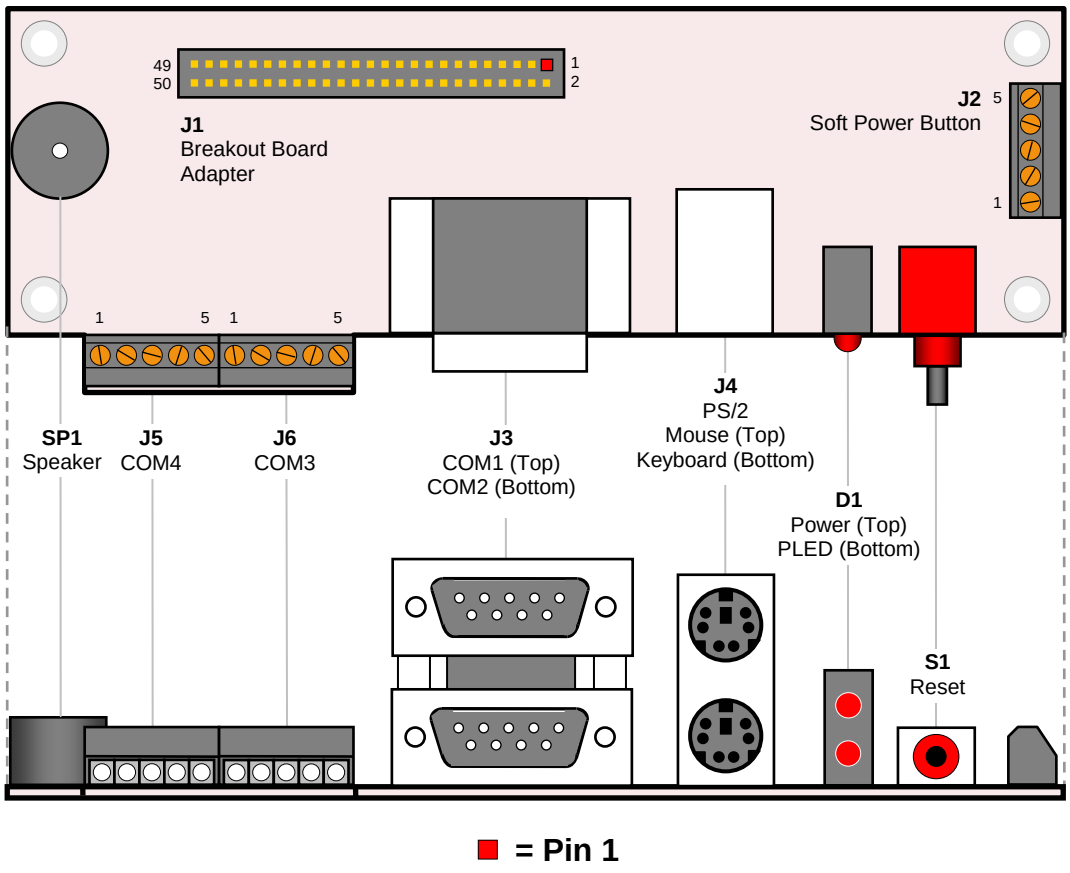


Figure 10. CBR-5009 Connectors

CBR-5009 CONNECTOR FUNCTIONS

Table 2: CBR-5009 Connector Functions

Connector / Component	Function	Part Number	Description
D1	Power and Programmable LEDs	Dialight 552-0211	LEDx2 T1 3/4 PC Mount Red/Red
J1	High Density Connector	FCI 98414-F06-50U	2mm, 50 pins, keyed, latching header
J2	Soft Power Button Input	Conta-Clip 10250.4	5 pin screw terminal
J3	COM1, COM2	Kycon K42-E9P/P-A4N	Dual stacked DB-9 male
J4	PS/2 Keyboard and Mouse	Kycon KMDG-6S/6S-S4N	Dual stacked PS/2 female
J5	COM4	Conta-Clip 10250.4	5 pin screw terminal
J6	COM3	Conta-Clip 10250.4	5 pin screw terminal
S1	Reset Button	E-Switch 800SP9B7M6RE	Right angle momentary switch
SP1	Speaker	Challenge Electronics DBX05	Miniature PC speaker

CBR-4004 CONNECTORS

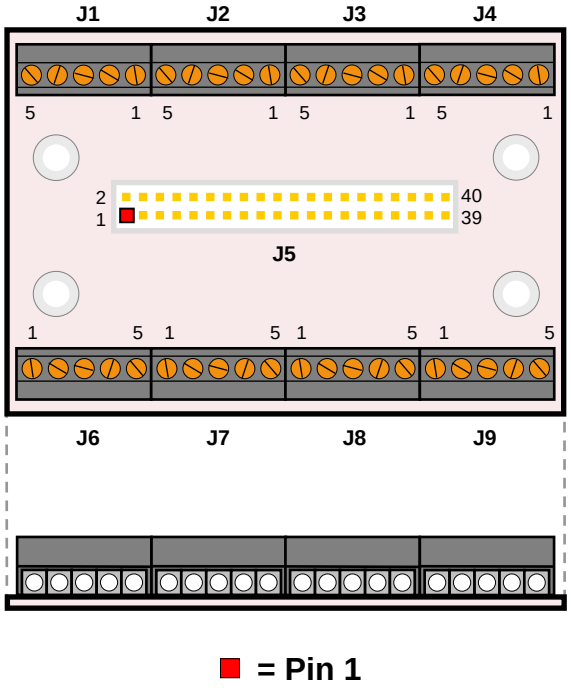


Figure 11. CBR-4004 Connectors

CBR-4004 connector functions depend on the I/O connector to which it is attached, J15 or J23. See Table 6 (J15) or Table 7 (J23) for details.

Jumper Blocks

JUMPERS AS-SHIPPED CONFIGURATION

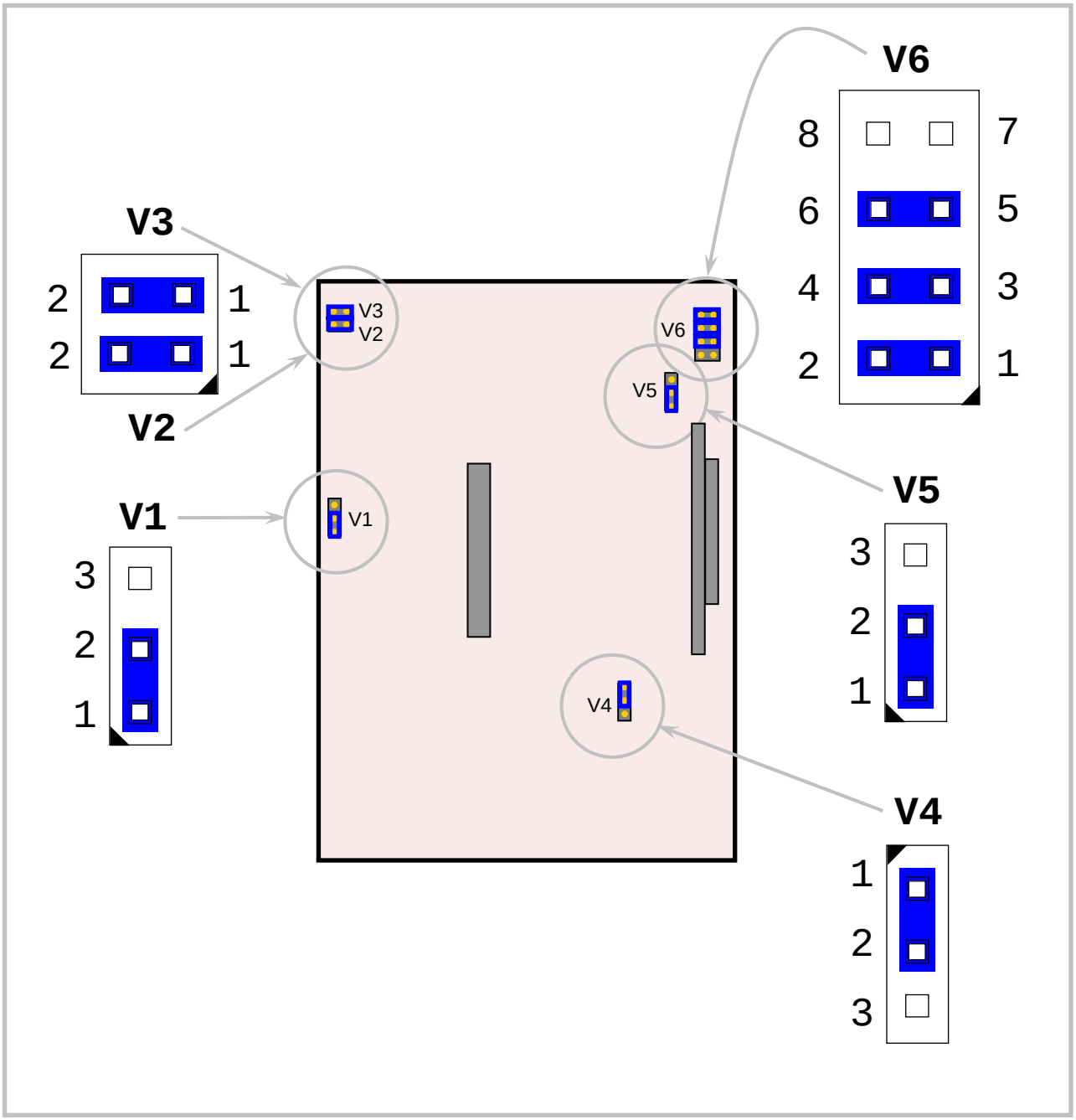


Figure 12. Jumper Block Locations

JUMPER SUMMARY

Table 3: Jumper Summary

Jumper Block	Description	As Shipped	Page
V1	**CMOS RAM and Real Time Clock Erase** [1-2] In – Normal [2-3] In – Erase CMOS RAM and real-time clock	[1-2] In (Normal)	29
V2[1-2]	**COM3 RS-485 Termination** In – 100 Ohm terminated Out – COM3 Not terminated	In	36
V3[3-4]	**COM4 RS-485 Termination** In – 100 Ohm terminated Out – COM4 Not terminated	In	36
V4	**CRT and TV Select** [1-2] In – CRT [2-3] In – TV	[1-2] In (CRT)	43
V5	**Reset Select** [1-2] In – Generated [2-3] In – Power button The EBX-22 requires activation of the soft power button to power up. Installing a jumper on pins [1-2] causes the EBX-22 to create its own soft power pulse automatically when power is applied. See page 10 for details.	[1-2] In (Generated)	–
V6[1-2]	**CompactFlash Master Selector** In – CompactFlash module is IDE master Out – CompactFlash module is IDE slave	In	41
V6[3-4]	**Video BIOS Selector** In – Primary video BIOS selected Out – Secondary video BIOS selected The secondary video BIOS is field-upgradeable using the FBU utility. See the EBX-22 support page for more information.	In	43
V6[5-6]	**Reserved** In – Normal operation Out – Factory use only This jumper should not be removed. If you hear a low-high beep tone and the EBX-22 appears to be failing to boot, verify that this jumper is properly installed.	In	–
V6[7-8]	**Reserved**	–	–

Power Supply

POWER CONNECTORS

Main power is applied to the EBX-22 through an EPIC-style 10-pin polarized connector at location J6.

Warning! To prevent severe and possibly irreparable damage to the system, it is critical that the power connectors are wired correctly. Make sure to use both +5VDC pins and all ground pins to prevent excess voltage drop.

Table 4: Main Power Connector Pinout

J6 Pin	Signal Name	Description
1	PS_ON	Soft Power Off
2	GND	Ground
3	GND	Ground
4	+12VDC	Power Input
5	+3.3VDC	Power Input
6	+5VSB	5V Standby
7	+5VDC	Power Input
8	+5VDC	Power Input
9	-12VDC	Power Input
10	GND	Ground

Note The +3.3VDC, +12VDC and -12VDC inputs on the main power connector are only required for PC/104-*Plus* and PC/104 expansion modules that require these voltages.

POWER REQUIREMENTS

The EBX-22 requires only +5.0 volts (±5%) for proper operation. The voltage required for the RS-232 ports and analog input sections are generated with a DC/DC converter. Low-voltage supply circuits provide power to the CPU and other on-board devices.

The exact power requirement of the EBX-22 depends on several factors, including memory configuration, CPU speed, peripheral connections, type and number of expansion modules and attached devices. For example, PS/2 keyboards typically draw their power directly from the EBX-22, and driving long RS-232 lines at high speed can increase power demand.

LITHIUM BATTERY

Warning! To prevent shorting, premature failure or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of used batteries promptly.

Normal battery voltage should be at least 3.0V. If the voltage drops below 3.0V, contact the factory for a replacement (part number HB3/0-1). The life expectancy under normal use is approximately 10 years.

VOLTAGE ALERT INTERRUPT

The EBX-22 can be configured to generate an interrupt if the 5V power rail exceeds 5.25V or drops below 4.75V. These voltage thresholds conform to the power supply recommendation of 5V +/- 5%. The voltage alert interrupt is enabled in CMOS Setup on the Board tab. Interrupts available for this purpose are IRQ 3, 4, 5, and 10. (The NMI, non-maskable interrupt, setting is reserved for future use).

Note: The IRQ for voltage and temperature monitoring is shared. When the Voltage or Temperature IRQ option is set, the selected IRQ will apply to both voltage and temperature monitoring if they are enabled.

CPU

The VIA Eden is an extremely low power consumption (7W at 1 GHz) x86 microprocessor with a maximum operating frequency of 1.2 GHz and bus speeds up to 800 mega-transfers per second (MT/s). The VIA Eden features two 64 KB Level 1 caches, one 128 KB Level 2 cache, and DDR2 SDRAM support.

System RAM

Compatible Memory Modules

The EBX-22 accepts one 240-pin SODIMM memory module with the following characteristics:

- Size Up to 1GB
- Voltage 1.8V
- Type PC2-4200 compatible (DDR2 533 MHz)

CMOS RAM

Clearing CMOS RAM

A jumper may be installed into V1[2-3] to erase the contents of the CMOS RAM and the Real-Time Clock. When clearing CMOS RAM:

1. Power off the EBX-22.
2. Remove the jumper from V1[1-2], install it on V1[2-3] and leave it for four seconds.
3. Move the jumper to back to V1[1-2].
4. Power on the EBX-22.

CMOS Setup Defaults

The EBX-22 permits users to modify not only the CMOS settings, but the defaults as well. This allows the system to boot up with user-defined settings if CMOS RAM is cleared or corrupted. All CMOS Setup defaults can be changed, except the time and date. The CMOS Setup defaults can be updated with the Flash BIOS Update (FBU) utility (version 3.11 or later), available from the General BIOS Information page.

Warning! If the CMOS Setup default settings make the system unbootable and prevents you from entering CMOS Setup, the EBX-22 needs to be serviced by the factory.

Default CMOS RAM Setup Values

After the CMOS RAM is cleared, the system will load default CMOS RAM parameters the next time the board is powered on. The default CMOS RAM setup values are used in order to boot the system whenever the main CMOS RAM values are blank, or when the system battery is dead or has been removed from the board.

SAVING CMOS SETUP PARAMETERS AS CUSTOM DEFAULTS

To save custom CMOS defaults, perform the following steps.

1. Configure CMOS Setup to your preferred custom default settings.
2. Install DOS onto one of the devices that has been configured as a boot device, and copy FBU to the device.
3. Boot the EBX-22 from this device. (During the early boot cycle, press the **B** key to access the boot menu, and select the DOS drive.)
4. Run FBU and select **Save CMOS contents**. A file named CMOS.BIN is created and saved to the floppy.
5. Select the FBU option **Load Custom CMOS defaults**. A directory of the floppy is displayed.
6. Select the CMOS.BIN file and press the **P** key to program the new CMOS defaults.
7. Reboot the system from the hard disk. The custom CMOS parameters are now saved as defaults.

Real Time Clock

The EBX-22 features a battery-backed 146818-compatible real-time clock/calendar chip. Under normal battery conditions, the clock maintains accurate timekeeping functions when the board is powered off.

SETTING THE CLOCK

CMOS Setup (accessed by pressing the Delete key during a system boot) can be used to set the time/date of the real-time clock.

Utility I/O Connectors

A number of interfaces on the EBX-22 are grouped together and made accessible through utility I/O connectors J14, J15, and J23. Cables and boards are available from VersaLogic that provide discrete connectors for each of the interfaces; however, you can create custom cables that surface only the interfaces required by your application.

J14 I/O Connector

The 50-pin I/O connector (J14) incorporates the COM ports, PS/2 keyboard and mouse, programmable LED, reset button, soft power reset, and speaker interfaces. Table 5 illustrates the function of each pin.

Table 5: J14 I/O Connector Pinout

J14 Pin	CBR-5009B Connector	Pin	Signal	
1	**COM1**	1	Data Carrier Detect	
2	**J3**	6	Data Set Ready	
3	Top DB9	2	Receive Data	
4		7	Request to Send	
5		3	Transmit Data	
6		8	Clear to Send	
7		4	Data Terminal Ready	
8		9	Ring Indicator	
9		5	Ground	
10	**COM2**	1	Data Carrier Detect	
11	**J3**	6	Data Set Ready	
12	Bottom DB9	2	Receive Data	
13		7	Request to Send	
14		3	Transmit Data	
15		8	Clear to Send	
16		4	Data Terminal Ready	
17		9	Ring Indicator	
18		5	Ground	
	COM3		**RS-232**	**RS-422/485**
19	**J6**	1	Ground	Ground
20		5	RTS	TxD+
21		4	TXD	TxD-
22		–	Ground	Ground
23		2	RXD	RxD-
24		3	CTS	RxD+
25		–	Ground	Ground

J14 Pin	CBR-5009B Connector	Pin	Signal	
	COM4		**RS-232**	**RS-422/485**
26	**J5**	1	Ground	Ground
27		5	RTS	TxD+
28		4	TXD	TxD-
29		–	Ground	Ground
30		2	RXD	RxD-
31		3	CTS	RxD+
32		–	Ground	Ground
33	**Mouse**	4	+5.0V (Protected)	
34	**J4**	1	Mouse Data	
35	Top	3	Ground	
36		5	Mouse Clock	
37	**PBRESET**	1	Pushbutton Reset	
38	**S1**	2	Ground	
39	**Soft Power**	1	Ground	
40	**Button J2**	2	External Wake	
41	–	–	Ground	
42		–	Not connected	
43	**Keyboard**	4	+5.0V (Protected)	
44	**J4**	1	Keyboard Data	
45	Bottom	3	Ground	
46		5	Keyboard Clock	
47	**PLED**	1	+5.0V (Protected)	
48	**D1**	2	Programmable LED	
49	**Speaker**	1	+5.0V (Protected)	
50	**SP1**	2	Speaker Drive	

J15 I/O CONNECTOR

The 40-pin I/O connector (J15) incorporates 16 digital I/O channels, eight analog channels, a reset, three PWM outputs, and four general purpose I/O lines. Table 6 shows the function of each pin.

Table 6: J15 I/O Connector Pinout

J15 Pin	Signal	CBR-4004 Connector	CBR-4004 Pin (Signal)
1	TAC_IN 1	**J1 General Purpose I/O**	5 (IO1)
2	TAC_IN 2		4 (IO2)
3	TAC_IN 3		3 (IO3)
4	PLD_CLK		2 (IO4)
5	GND		1 (GND1)
6	PWM_OUT 1	**J2 PWM Output**	5 (IO5)
7	PWM_OUT 2		4 (IO6)
8	PWM_OUT 3		3 (IO7)
9	NC		2 (IO8)
10	GND		1 (GND1)
11	Digital I/O 0	**J3 Digital IO**	5 (IO9)
12	Digital I/O 1		4 (IO10)
13	Digital I/O 2		3 (IO11)
14	Digital I/O 3		2 (IO12)
15	GND		1 (GND2)
16	Digital I/O 4	**J4 Digital IO**	5 (IO13)
17	Digital I/O 5		4 (IO14)
18	Digital I/O 6		3 (IO15)
19	Digital I/O 7		2 (IO16)
20	GND		1 (GND2)
21	Digital I/O 8	**J6 Digital IO**	1 (IO17)
22	Digital I/O 9		2 (IO18)
23	Digital I/O 10		3 (IO19)
24	Digital I/O 11		4 (IO20)
25	Pushbutton Reset		5 (GND3/PBRST#)
26	Digital I/O 12	**J7 Digital IO**	1 (IO21)
27	Digital I/O 13		2 (IO22)
28	Digital I/O 14		3 (IO23)
29	Digital I/O 15		4 (IO24)
30	GND		5 (GND3)
31	ADCH0	**J8 Analog**	1 (IO25)
32	ADCH1		2 (IO26)
33	ADCH2		3 (IO27)
34	ADCH3		4 (I028)
35	GND		5 (GND4)
36	ADCH4	**J9 Analog**	1 (IO29)
37	ADCH5		2 (IO30)
38	ADCH6		3 (IO31)
39	ADCH7		4 (IO32)
40	GND		5 (GND4)

J23 I/O CONNECTOR

The 40-pin I/O connector (J23) incorporates the USB4 interface, 16 digital I/O channels, and the audio interface. Table 7 illustrates the function of each pin.

Table 7: J23 I/O Connector Pinout

J23 Pin	Signal	CB-4004 Connector	CBR-4004 Signal
1	GND	**J1 USB4**	5 (IO1)
2	USB4_PWR		4 (IO2)
3	USBDT4+		3 (IO3)
4	USBDT4-		2 (IO4)
5	GND		1 (GND1)
6	PLD_GPIO 0	**J2 PLD_GPIO**	5 (IO5)
7	PLD_GPIO 1		4 (IO6)
8	PLD_GPIO 2		3 (IO7)
9	GND		2 (IO8)
10	GND		1 (GND1)
11	Digital I/O 16	**J3 Digital IO**	5 (IO9)
12	Digital I/O 17		4 (IO10)
13	Digital I/O 18		3 (IO11)
14	Digital I/O 19		2 (IO12)
15	GND		1 (GND2)
16	Digital I/O 20	**J4 Digital IO**	5 (IO13)
17	Digital I/O 21		4 (IO14)
18	Digital I/O 22		3 (IO15)
19	Digital I/O 23		2 (IO16)
20	GND		1 (GND2)
21	Digital I/O 24	**J6 Digital IO**	1 (IO17)
22	Digital I/O 25		2 (IO18)
23	Digital I/O 26		3 (IO19)
24	Digital I/O 27		4 (IO20)
25	GND		5 (GND3/PBRST#)
26	Digital I/O 28	**J7 Digital IO**	1 (IO21)
27	Digital I/O 29		2 (IO22)
28	Digital I/O 30		3 (IO23)
29	Digital I/O 31		4 (IO24)
30	GND		5 (GND3)
31	NC	**J8 Audio Out**	1 (IO25)
32	AUDOUTR		2 (IO26)
33	GND		3 (IO27)
34	AUDOUTL		4 (I028)
35	GND		5 (GND4)
36	NC	**J9 Audio In**	1 (IO29)
37	AUDINR		2 (IO30)
38	NC		3 (IO31)
39	AUDINL		4 (IO32)
40	GND		5 (GND4)

IDE

One IDE interface is available to connect up to two IDE devices, such as hard disks and CD-ROM drives. If the on-board CompactFlash is configured for use, only one other IDE device can be attached to the IDE controller. Connector J22 provides the interface to the IDE controller. Jumper V6[1-2] determines if the CompactFlash plugged into J20 is the master device or slave. Use CMOS Setup to specify the drive parameters of the attached drives.

Warning! Cable length must be 18" or less to maintain proper signal integrity.

Table 8: IDE Hard Drive Connector Pinout

J22 Pin	Signal Name	Function	J22 Pin	Signal Name	Function
1	Reset-	Reset signal from CPU	23	DIOW	I/O write
2	Ground	Ground	24	Ground	Ground
3	DD7	Data bus bit 7	25	DIOR	I/O read
4	DD8	Data bus bit 8	26	Ground	Ground
5	DD6	Data bus bit 6	27	IORDY	I/O ready
6	DD9	Data bus bit 9	28	Ground	Ground
7	DD5	Data bus bit 5	29	DMACK-	DMA acknowledge
8	DD10	Data bus bit 10	30	Ground	Ground
9	DD4	Data bus bit 4	31	INTRQ	Interrupt request
10	DD11	Data bus bit 11	32	NC	No connection
11	DD3	Data bus bit 3	33	DA1	Device address bit 1
12	DD12	Data bus bit 12	34	PDIAG	Passed diagnostics
13	DD2	Data bus bit 2	35	DA0	Device address bit 0
14	DD13	Data bus bit 13	36	DA2	Device address bit 2
15	DD1	Data bus bit 1	37	CS0	Chip select 0
16	DD14	Data bus bit 14	38	CS1	Chip select 1
17	DD0	Data bus bit 0	39	IDE_LED	IDE LED
18	DD15	Data bus bit 15	40	Ground	Ground
19	Ground	Ground	41	Power	+5.0V
20	NC	Key	42	Power	+5.0V
21	PDMARQ	DMA request	43	Ground	Ground
22	Ground	Ground	44	NC	No connection

SATA Ports

The EBX-22 provides two serial ATA (SATA) ports, which communicate at a rate of up to 1.5 gigabits per second (SATA 1). The SATA connectors at locations J8 and J10 are standard 7-pin straight SATA connectors with friction latching. Power to SATA drives is supplied by the ATX power supply. Note that the standard SATA drive power connector is different than the common 4-pin Molex connector used on IDE drives. Most current ATX power supplies provide SATA connectors, and many SATA drives provide both types of power connectors. If the power supply you are using does not provide SATA connectors, adapters are available.

Table 9: SATA Port Pinout

J8 or J10 Pin	Signal Name	Function
1	GND	Ground
2	TX+	Transmit +
3	TX-	Transmit -
4	GND	Ground
5	RX-	Receive -
6	RX+	Receive +
7	GND	Ground

Note The mating connector on some SATA data cables may interfere with the proper seating of a PC/104-*Plus* (PCI) expansion board at connector J17. The SATA specification does not specify exterior dimensions for connector housings, and some manufacturers make wider housings than others. The 3M 5602 Series straight SATA connector is 0.22 in. wide and will interfere less with the PC/104-*Plus* card. Even with thinner SATA cables, you may need to ease the cable(s) away from the PC/104-*Plus* connector to seat the expansion board completely.

Serial Ports

The EBX-22 features four on-board 16550-based serial channels located at standard PC I/O addresses. COM1 and COM2 are RS-232 (115.2K baud) serial ports. IRQ lines are chosen in CMOS Setup. COM ports can share interrupts with other COM ports, but not with other devices.

COM3 and COM4 can be operated in RS-232 4-wire, RS-422 or RS-485 modes. Additional non-standard baud rates are also available (programmable in the normal baud registers) of up to 460k baud. IRQ lines are chosen in the CMOS Setup.

Each COM port can be independently enabled, disabled, or assigned a different I/O base address in CMOS Setup.

COM Port Configuration

There are no configuration jumpers for COM1 and COM2 since they only operate in RS-232 mode. Use CMOS Setup to select between RS-232 4-wire, RS-422, and RS485 operating modes for COM3 and COM4.

Jumper V2 is used to enable the RS-422/485 termination resistor for COM3. Jumper V3 is used to enable the RS-422/485 termination resistor for COM4. The termination resistor should be enabled for RS-422 and the RS-485 endpoint station. It should be disabled for RS-232 and the RS-485 intermediate station.

If RS-485 mode is used, the differential twisted pair (TxD+/RxD+ and TxD-/RxD-) is formed by connecting both transmit and receive pairs together. For example, on CBR-5009 connectors J6 and J5, the TxD+/RxD+ signal is formed by connecting pins 3 and 5, and the TxD-/RxD- signal is formed by connecting pins 2 and 4.

COM3 / COM4 RS-485 Mode Line Driver Control

The EBX-22 features automatic RS-485 direction control for COM3 and COM4. The purpose of this function is to save the effort of RS-485 direction control in software. The direction control signal RTS is used to tri-state the transmitter when no other data is available, so that other nodes can use the shared lines.

RS-485 direction control is set using the Serial Port 3 > Mode and Serial Port 4 > Mode parameters in CMOS Setup. To enable manual direction control, set the COM port mode to RS485 ManuFC; to enable auto direction control, set the parameter to RS485 AutoFC. Manual direction control is configured by asserting the RTS handshake line. Asserting the RTS handshake line puts the RS-485 port in transmit mode; de-asserting the line puts it in receive mode.

SERIAL PORT CONNECTORS

See the *Connector Location Diagrams* on pages 21 for connector and cable information. The pinouts of the DB9M connectors apply to the serial connectors on the VersaLogic breakout board CBR-5009.

These connectors use IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 10: COM1-2 Pinout – CBR-5009 Connector J3

COM1	COM2	
Top DB9 J3 Pin	Bottom DB9 J3 Pin	RS-232
1	10	DCD
2	11	RXD*
3	12	TXD*
4	13	DTR
5	14	Ground
6	15	DSR
7	16	RTS
8	17	CTS
9	18	RI

Table 11: COM3-4 Pinout – CBR-5009 Connectors J5-6

COM3	COM4			
J6 Pin	J5 Pin	RS-232	RS-422	RS-485
1	1	Ground	Ground	Ground
2	2	RXD	RxD-	RxD-
3	3	CTS	RxD+	RxD+
4	4	TXD	TxD-	TxD-
5	5	RTS	TxD+	TxD+

Parallel/Floppy Port

PARALLEL PORT OPERATION

The EBX-22 includes a standard bi-directional/EPP/ECP compatible LPT port (connector J29) that resides at the PC standard address of 378h. The port can be enabled or disabled and interrupt assignments can be made via CMOS Setup. The LPT mode is also set via CMOS Setup.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 12: LPT Parallel/Floppy Port Pinout

J29 Pin	Centronics Signal	Signal Direction
1	Strobe	Out
2	Auto feed	Out
3	Data bit 0	In/Out
4	Printer error	In
5	Data bit 1	In/Out
6	Reset	Out
7	Data bit 2	In/Out
8	Select input	Out
9	Data bit 3	In/Out
10	Data bit 4	In/Out
11	Data bit 5	In/Out
12	Data bit 6	In/Out
13	Data bit 7	In/Out
14	Ground	—
15	Acknowledge	In
16	Ground	—
17	Port busy	In
18	Ground	—
19	Paper end	In
20	Printer select	In

PARALLEL PORT FLOPPY DISK

The parallel port on the EBX-22 can be used as a floppy disk interface. To use this feature:

1. In CMOS Setup, select SIO > Parallel Port (J29) > Mode = [Floppy Drive (via CBL-2501)].
2. Connect the floppy drive to connector J29 using the CBR-2501/CBR-2003 combination cables.

PS/2 Keyboard and Mouse

A standard PS/2 keyboard and mouse interface is accessible through connector J4 of the VersaLogic breakout board, CBR-5009. The breakout board is connected to connector J14 of the EBX-22. The 5V power provided to the keyboard and mouse is protected by a 1 Amp fuse.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 13: PS/2 Mouse and Keyboard Pinout

CBR-5009 J4 Top Pin	Signal	Description
1	MSDATA	Mouse Data
2	–	No Connection
3	GND	Ground
4	MKPWR	+5.0V (Protected)
5	MSCLK	Mouse Clock
6	–	No Connection
CBR-5009 J4 Bottom Pin	**Signal**	**Description**
1	KBDATA	Keyboard Data
2	–	No Connection
3	GND	Ground
4	MKPWR	+5.0V (Protected)
5	KBCLK	Keyboard Clock
6	–	No Connection

USB

The USB interface on the EBX-22 is UHCI (Universal Host Controller Interface) and EHCI (Enhance Host Controller Interface) compatible, which provides a common industry software/hardware interface. There are six USB ports. Four standard USB Series A sockets (USB0-3) are located on the base board at locations J3, J4, J9, and J11. USB4 is available on the CBR-4004 I/O board as a screw terminal connector at location J1. And USB5 is a 10-pin solid state drive (SSD) interface on the base board at location J13.

These connectors use IEC 61000-4-2-rated TVS components to help protect against ESD damage.

BIOS CONFIGURATION

Three USB 1.1 controllers (UHCI) use PCI interrupt INTA#, INTB#, and INTC#. One USB 2.0 (EHCI) controller uses PCI interrupt INTD#. CMOS Setup is used to select the IRQ line routed to each PCI interrupt line.

USB SOLID STATE DRIVE CONNECTOR

The USB SSD connector J13 accepts Intel Z-U130 low profile or equivalent drives. These drives are available in capacities of 1 GB, 2 GB and 4 GB. The following table shows the pinout of the J13 connector.

Table 14: USB5 Solid State Drive Pinout

J13 Pin	Signal Name	Function
1	USB_PWR	+5.0V (Protected)
2	NC	No Connection
3	USBDT5-	USB5 Data -
4	NC	No Connection
5	USBDT5+	USB5 Data +
6	NC	No Connection
7	GND	Ground
8	NC	No Connection
9	Key	Pin Removed
10	LED#	LED Output

The USB SSD can be secured to the base board using 4.5 mm x 5 mm x M2.5 thread standoff, such as the RAF Electronic Hardware part M2100-2545-SS.

CompactFlash

Connector J20 provides a socket for a Type I or Type II CompactFlash (CF) module. This IDE based interface operates on the same channel than the IDE interface at connector J22. The CF interface supports operation in DMA mode.

The following CF modules have been tested and qualified as bootable devices by VersaLogic. Part numbers with a suffix of -3500 are RoHS-compliant.

Table 15. Qualified Bootable CF Modules

Manufacturer	Density	Mfg Part Number
Hagiwara	1 GB	CF1-1GMDG(H00AA)
Hagiwara	512 MB	CF1-512MDG(H00AA)
Silicon Systems	128 MB	SSD-C12M-3012
Silicon Systems	128 MB	SSD-C12M-3500
Silicon Systems	256 MB	SSD-C25M-3012
Silicon Systems	256 MB	SSD-C25MI-3012
Silicon Systems	256 MB	SSD-C25M-3500
Silicon Systems	256 MB	SSD-C25MI-3500
Silicon Systems	512 MB	SSD-C51M-3012
Silicon Systems	512 MB	SSD-C51MI-3012
Silicon Systems	512 MB	SSD-C51M-3500
Silicon Systems	512 MB	SSD-C51MI-3500
Silicon Systems	1 GB	SSD-C01G-3012
Silicon Systems	1 GB	SSD-C01G-3500
Silicon Systems	2 GB	SSD-C02G-3012
Silicon Systems	2 GB	SSD-C02GI-3012
Silicon Systems	2 GB	SSD-C02G-3500
Silicon Systems	4 GB	SSD-C04GI-3012

INSTALLING AN OPERATING SYSTEM ON COMPACTFLASH

Installing an operating system to a CF module is best performed using a USB CD-ROM drive.

1. Remove the jumper installed at V6[1-2]. Removing the jumper designates the CF as the slave IDE device. (Note: If you use an IDE CD-ROM drive instead of a USB drive, the CD-ROM drive must be the master and the CF the slave.)
2. Boot from the CD-ROM drive. (During the early boot cycle, press the **B** key to access the boot menu, and select the drive.)
3. Install the OS.

   After installing the OS, you may configure the CF to be the first boot device, which will reduce boot time.

Programmable LED

Connector J14 includes an output signal for attaching a software controlled LED. Connect the cathode of the LED to J14, pin 48; connect the anode to +5V. An on-board resistor limits the current to 15 mA when the circuit is turned on. A programmable LED is provided on the CBR-5009 breakout board.

To turn the LED on and off, set or clear bit D7 in I/O port 1D0h (or 1E0h). When changing the register, make sure not to alter the values of the other bits.

The following code examples show how to turn the LED on and off. Refer to page 69 for further information:

LED On

```
MOV    DX,1D0H
IN     AL,DX
OR     AL,80H
OUT    DX,AL
```

LED Off

```
MOV    DX,1D0H
IN     AL,DX
AND    AL,7FH
OUT    DX,AL
```

Note The LED is turned on by the BIOS during system startup. This causes the light to function as a "power on" indicator if it is not otherwise controlled by user code.

External Speaker

A miniature 8 ohm speaker can be connected between J14, pin 50 (SPKO*) and J4, pin 49 (MKPWR). A speaker is provided on the CBR-5009 breakout board.

Push-Button Reset

Connector J14 includes an input for a push-button reset switch. Shorting J14, pin 37 to ground causes the EBX-22 to reboot.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

A reset button is provided on the CBR-5009 breakout board.

Video Interface

An on-board video controller integrated into the chipset provides high performance video output for the EBX-22. Video output options include SVGA analog, LVDS flat panel, and DVI/HDMI.

CONFIGURATION

The video interface uses PCI interrupt INTA#. CMOS Setup is used to select the IRQ line routed to INTA#. The EBX-22 uses shared memory architecture. This allows the video controller to use variable amounts of system DRAM for video RAM. The amount of RAM used for video is set with a CMOS Setup option.

The EBX-22 supports three types of video output, SVGA, LVDS Flat Panel Display and DVI/HDMI. A CMOS Setup option is used to select which output is enabled after POST.

VIDEO BIOS SELECTION

Jumper V6[3-4] can be removed to allow the system to boot the secondary video BIOS. Unlike the primary video BIOS, the secondary video BIOS can be reprogrammed in the field. Using the primary video BIOS, screen resolutions of up to 1600 x 1200 at 32 bits are available. (These maximums may be reduced if both outputs are enabled.) Using the secondary video BIOS enables the LVDS output. These may be combined with CRT or DVI (but not both) at a matching resolution.

SVGA OUTPUT CONNECTOR

See the diagram on page 21 for the location of connector J7. An adapter cable, part number CBR-1201, is available to translate J7 into a standard 15-pin D-Sub SVGA connector. Jumper V4 is used to select between CRT (default) and analog TV output. Setting the jumper to TV (V4[2-3]) produces YPbPr (component) video output and requires the use of a 15-pin D-Sub to component video adapter cable.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 16: Video Output Pinout

J7 Pin	Signal Name	Function	Mini DB15 Pin
1	GND	Ground	6
2	RED	Red Video	1
3	GND	Ground	7
4	GREEN	Green Video	2
5	GND	Ground	8
6	BLUE	Blue Video	3
7	GND	Ground	5
8	HSYNC	Horizontal Sync	13
9	GND	Ground	10
10	VSYNC	Vertical Sync	14
11	ID0	Monitor ID Bit 0	11
12	SDA	DDC Serial Data Line	12

LVDS Flat Panel Display Connector

The integrated LVDS Flat Panel Display provided through connector J19 on the EBX-22 is an ANSI/TIA/EIA-644-1995 specification-compliant interface. It can support up to 24 bits of RGB pixel data plus 3 bits of timing control (HSYNC/VSYNC/DE) on the 4 differential data output pairs. The LVDS clock frequency ranges from 25 MHz to 112 MHz.

CMOS Setup provides several options for standard LVDS Flat Panel types. If these options do not match the requirements of the panel you are attempting to use, contact Support@VersaLogic.com for a custom video BIOS.

The 3.3V power provided to pins 19 and 20 of J19 is protected by a 1 Amp fuse.

See the connector location diagram on page 21 for pin and connector location information.

Table 17: LVDS Flat Panel Display Pinout

J19 Pin	Signal Name	Function
1	GND	Ground
2	NC	Not Connected
3	LVDSA3	Diff. Data 3 (+)
4	LVDSA3#	Diff. Data 3 (-)
5	GND	Ground
6	LVDSCLK0	Differential Clock (+)
7	LVDSCLK0#	Differential Clock (-)
8	GND	Ground
9	LVDSA2	Diff. Data 2 (+)
10	LVDSA2#	Diff. Data 2 (-)
11	GND	Ground
12	LVDSA1	Diff. Data 1 (+)
13	LVDSA1#	Diff. Data 1 (-)
14	GND	Ground
15	LVDSA0	Diff. Data 0 (+)
16	LVDSA0#	Diff. Data 0 (-)
17	GND	Ground
18	GND	Ground
19	+3.3V	+3.3V (Protected)
20	+3.3V	+3.3V (Protected)

COMPATIBLE LVDS PANEL DISPLAYS

The following flat panel displays are reported to work properly with the integrated graphics video controller chip used on the EBX-22.

Table 18: Compatible Flat Panel Displays

Manufacturer	Model Number	Panel Size	Resolution	Interface	Panel Technology
eVision Displays	xxx084S01 series	8.4”	800 x 600 18-bit	LVDS	TFT
au Optronix	B084SN01	8.4”	800 x 600 18-bit	LVDS	TFT
eVision Displays	xxx104S01 series	10.4”	800 x 600 18-bit	LVDS	TFT
au Optronix	B104SN01	10.4”	800 x 600 18-bit	LVDS	TFT
eVision Displays	xxx141X01 series	14.1”	1024 x 768 18-bit	LVDS	TFT
Sharp	LQ121S1LG411	12.1”	800 x 600 18-bit	LVDS	TFT

HIGH-DEFINITION MULTIMEDIA INTERFACE

The EBX-22 incorporates a High-Definition Multimedia Interface (HDMI) that supports most PC video formats, including standard, enhanced, or high-definition video on a single cable. (Audio is not supported in the EBX-22 HDMI implementation.) HDMI encodes video data into transition minimized differential signaling (TMDS) for digital transmission. Connector J24 is a standard HDMI Type A connector.

Table 19: HDMI Pinout

J24 Pin	Signal Name	Function
1	DATA2+	Data 2 (+)
2	DATA2SHIELD	Ground
3	DATA2-	Data 2 (-)
4	DATA1+	Data 1 (+)
5	DATA1SHIELD	Ground
6	DATA1-	Data 1 (-)
7	DATA0+	Data 0 (+)
8	DATA0SHIELD	Ground
9	DATA0-	Data 0 (-)
10	CLOCK+	Clock (+)
11	CLOCKSHIELD	Ground
12	CLOCK-	Clock (-)
13	NC	No connection
14	NC	No connection
15	SCL	Serial clock
16	SDA	Serial data
17	DCD/CEC_GND	Ground
18	+5V	+5.0V (Protected)
19	NC	No connection

CONSOLE REDIRECTION

The EBX-22 can be operated without using the on-board video output by redirecting the console to a serial communications port. CMOS Setup and some operating systems such as DOS can use this console for user interaction.

Console redirection settings are configured on the Features tab of CMOS Setup. The default setting causes the console not to be redirected to COM1 unless a signal (a Ctrl-C character) is detected from the terminal. Console redirection can also be set to Always or Never. You can direct console output to any COM port.

Notes on console redirection:

- When console redirection is enabled, you can access CMOS Setup by pressing and holding down Ctrl-C.
- The decision to redirect the console is made early in BIOS execution and cannot be changed later.
- The redirected console uses 115200 baud, 8 data bits, 1 stop bit, no parity, and no flow control.
- The default console redirection setting is Auto. The default can be reloaded without entering BIOS setup by discharging CMOS contents.

Null Modem

The following diagram illustrates a typical DB9 to DB9 RS-232 null modem adapter. Pins 7 and 8 are shorted together on each connector. Unlisted pins have no connection.

```
System 1  <-->  System 2
Name Pin        Pin Name
-----------------------
TX    3   <-->   2  RX
RX    2   <-->   3  TX
RTS   7   <-->   1  DCD
CTS   8
DSR   6   <-->   4  DTR
DCD   1   <-->   7  RTS
                 8  CTS
DTR   4   <-->   6  DSR
```

Ethernet Interface

The EBX-22 features two Intel 82551ER Fast Ethernet controllers on-board. While these controllers are not NE2000-compatible, they are widely supported. Drivers are readily available to support a variety of operating systems.

BIOS CONFIGURATION

Each Ethernet controller can be enabled or disabled in CMOS Setup. Ethernet interface 0 (J12) uses PCI interrupt INTC#. CMOS Setup is used to select the IRQ line routed to each PCI interrupt line. Ethernet interface 1 (J5) uses PCI interrupt INTD#.

STATUS LED

Each Ethernet controller has a two-colored LED located next to its RJ-45 connector to provide an indication of the Ethernet status as follows:

Green LED (Link):

- ON — Active Ethernet cable plugged in
- OFF — Active cable not plugged in or cable not plugged into active hub

Yellow LED (Activity):

- ON — Activity detected on cable
- OFF — No Activity detected on cable

ETHERNET CONNECTOR

Board-mounted RJ-45 connectors are provided to make connections with Category 5 Ethernet cables. The 82551ER Ethernet controller auto-detects 10BaseT/100Base-TX connectors.

These connectors use IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 20: RJ45 Ethernet Pinout

J5/J12 Pin	Signal Name	Function
1	T+	Transmit Data +
2	T-	Transmit Data -
3	R+	Receive Data +
4	IGND	Isolated Ground
5	IGND	Isolated Ground
6	R-	Receive Data -
7	IGND	Isolated Ground
8	IGND	Isolated Ground

CPU Temperature Monitor

A thermometer circuit constantly monitors the die temperature of the CPU. This circuit can be used to detect over-temperature conditions which can result from heat sink failure or excessive ambient temperatures.

The EBX-22 can be configured to generate an interrupt when the temperature exceeds user-defined thresholds for CPU and board temperatures. CMOS Setup options on the Board tab are used to set temperature thresholds from 0 to 255°C. The temperature IRQ is also selected on the Board tab. Interrupts available are IRQ 3, 4, 5, and 10. (The NMI, non-maskable interrupt, setting is reserved for future use).

Note: The IRQ for voltage and temperature monitoring is shared. When the Voltage or Temperature IRQ option is set, the selected IRQ will apply to both voltage and temperature monitoring if they are enabled.

See the SMSC SCH3114 Super I/O Chip data sheet for information on reading and writing to the thermometer circuits.

Audio

The audio interface on the EBX-22 is implemented using the VIA VT1708 High Definition Audio Codec. This interface is AC'97 2.3 compatible. Drivers are available for most Windows-based operating systems. To obtain the most current versions, consult the EBX-22 product support page at **http://www.versalogic.com/private/Sidewindersupport.asp.**

J23 provides the line-level stereo input and line-level stereo output connection points. The outputs will drive any standard-powered PC speaker set.

SOFTWARE CONFIGURATION

The audio interface uses PCI interrupt INTB#. The CMOS setup screen is used to select the IRQ line routed to INTB#.

The audio controller can be disabled within the CMOS setup.

Table 21: Audio Pinout

J23 Pin	CBR-4004 J9 Pin	Signal Name	Function
37	2	AUDINR	Line-In Right
39	4	AUDINL	Line-In Left
40	5	GND	Ground
J23 Pin	**CBR-4004 J8 Pin**	**Signal Name**	**Function**
32	2	AUDOUTR	Line-Out Right
34	4	AUDOUTL	Line-Out Left
35	5	GND	Ground

Watchdog Timer

A watchdog timer circuit is included on the EBX-22 that resets the CPU if proper software execution fails or a hardware malfunction occurs.

ENABLING THE WATCHDOG

Bit D7 of the WDSET register (I/O port 1E0h) is used to enable or disable the watchdog from resetting the CPU on timer expiration. The EXP field (bits D6-D0) of the same register set the expiration time. The expiration time can be set to a maximum of just under 16 seconds (7Fh) and a minimum of 1 second (08h). The formula for determining the EXP code is given as:

Seconds x 8 = Decimal Value = Hex Value

For example, for an expiration time of 5.5 seconds:

5.5 x 8 = 44 = 2Ch (written to the EXP field of the WDSET register)

DISABLING THE WATCHDOG

Clearing bit D7 in the WDSET register (at I/O port 1E0h) disables the watchdog timer. No special procedure is required.

REFRESHING THE WATCHDOG

If the watchdog timer is enabled, software must periodically refresh the WDHOLD register at a rate faster than the timer is set to expire. (This is sometimes referred to as "petting" or "feeding" the watchdog.) To reset the timer, first write 55h to the WDHOLD register (I/O port 1E1h) followed by AAh to the same register.

WATCHDOG TIMER REGISTERS

WDSET (Read/Write) 1E0h

D7	D6	D5	D4	D3	D2	D1	D0
ENABLE	EXP6	EXP5	EXP4	EXP3	EXP2	EXP1	EXP0

Table 22: WDSET Register Bit Assignments

Bit	Mnemonic	Description
D7	ENABLE	**Watchdog Enable** – Enables and disables the watchdog timer reset circuit. 0 = Disabled 1 = Enabled
D6-D0	EXP	**Expiration Time –** These bits define the expiration time for the watchdog timer. The expiration time can be set from 1 to ~16 seconds, or from 08h to 7Fh. See Enabling the Watchdog.

WDHOLD (Read/Write) 1E1h

D7	D6	D5	D4	D3	D2	D1	D0
PET7	PET6	PET5	PET4	PET3	PET2	PET1	PET0

Table 23: WDHOLD Register Bit Assignments

Bit	Mnemonic	Description
D7-D0	PET	**Pet Watchdog** – If the watchdog timer is enabled, this register must be periodically refreshed at a rate faster than the timer is set to expire. The code sequence to hold off a reset is 55h, AAh.

Analog Input

The EBX-22 analog input interface uses a 12-bit A/D converter that accepts up to eight single-ended input signals. The converter features 500 kilo-samples per second (kSPS) conversion time, with an input range of 0 to +4.095V with 4096 steps at 0.001V each. A/D input capacitance is 33 pF. The absolute maximum input voltage is 4.395V (4.095V + 0.300V) and minimum input voltage -0.300V.

The EBX-22 A/D converter can be controlled three different ways, using an ADC state machine, the SPI interface, or the analog input "bit bang" registers. This section describes all three A/D conversion methods. The ADC state machine method constantly scans the analog chip for inputs.

Warning! Application of analog voltages greater than +4.395V can physically damage the converter.

EXTERNAL CONNECTIONS

Single-ended analog voltages are applied to connector J15 as shown in the following table.

Table 24: Analog Input Pinout

J15 Pin	Signal	Function	CBR-4004 Connector	CBR-4004 Pin (Signal)
31	ADCH0	Analog Input Channel 0	**J8 Analog**	1 (IO25)
32	ADCH1	Analog Input Channel 1		2 (IO26)
33	ADCH2	Analog Input Channel 2		3 (IO27)
34	ADCH3	Analog Input Channel 3		4 (I028)
35	GND	Ground		5 (GND4)
36	ADCH4	Analog Input Channel 4	**J9 Analog**	1 (IO29)
37	ADCH5	Analog Input Channel 5		2 (IO30)
38	ADCH6	Analog Input Channel 6		3 (IO31)
39	ADCH7	Analog Input Channel 7		4 (IO32)
40	GND	Ground		5 (GND4)

CALIBRATION

There are no calibration adjustments. Calibration, if desired, is accomplished by mathematical transformation in software.

BINARY FORMAT (0 TO +4.095V ONLY)

The full analog input range is divided into 4096 steps. The output code (0000h) is associated with an analog input voltage of 0 volts (ground). All codes are considered positive.

The following formulas are used for calculating analog and digital values:

$$Digital = \left[\frac{Analog}{Step} \right] \qquad Analog = Step \times Digital$$

Where:

Analog = Applied voltage

Digital = A/D conversion data

Step = 0.001V

Sample values are shown in the following table.

Table 25: Binary Data Format

0 to +4.096V Input Voltage	Hex	Decimal	Comment
+4.096V	–	–	Out of range
+4.095V	0FFFh	4095	Maximum voltage
+2.048V	0800h	2048	Half scale
+1.024V	0400h	1024	Quarter scale
+0.001V	0001h	1	1 LSB
0.000000	0000h	0	Zero (ground input)

ADC STATE MACHINE

Data Registers

The EBX-22 ADC state machine uses eight 16-bit registers for analog input, at even-numbered base addresses from I/O port 1C0h to 1CEh. The state machine continuously reads ADC channels in a “round robin” fashion and places the data in the 16-bit registers. It reads the eight channels approximately 40,000 times a second. To enable the ADC state machine, the ADC field (bits D1-D0) of the MODCON register (1DFh) must be set to 2h (see Table 44 for mode control settings). This is best done by a read-modify-write procedure since the other bits in the register control other devices.

Table 26 shows the addresses of all analog input registers.

Table 26: Analog Input 16-bit Register Addresses

Channel	Base Address	Register
Analog Input 0	1C0h	ADC0
Analog Input 1	1C2h	ADC1
Analog Input 2	1C4h	ADC2
Analog Input 3	1C6h	ADC3
Analog Input 4	1C8h	ADC4
Analog Input 5	1CAh	ADC5
Analog Input 6	1CCh	ADC6
Analog Input 7	1CEh	ADC7

ADC Data Register

ADCx (Read Only)

D15	D14	D13	D12	D11	D10	D9	D8
–	–	–	–	AD11	AD10	AD9	AD8

D7	D6	D5	D4	D3	D2	D1	D0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

The ADCx register is a 16-bit read register containing 12 bits of data from A/D conversion results. The four most significant bits are always 0.

Table 27: ADCx Bit Assignments

Bit	Mnemonic	Description
D15-D0	AD	**A/D Input Data** – These bits contain the 12-bit conversion results. Bits D15 through D12 are always 0.

ADC State Machine Code Example

The following code example illustrates the procedure for reading analog voltage from channel 0:

```
MOV   DX,1C0      ;Point to ADC0 register
IN    AX,DX       ;Read ADC0 register
```

ANALOG INPUT USING THE SPI INTERFACE

See SPI Interface for a description of the EBX-22 SPI interface and registers.

Initiating an Analog Conversion Using the SPI Interface

The following procedure can be used to initiate an analog conversion using the SPI interface.

1. Write 15h to the SPICONTROL register (I/O address 1D8h) – This value configures the SPI port to select the on-board A/D converter, 16-bit frame length, low SCLK idle state, rising edge SCLK edge, and automatic slave select.
2. Write 30h to the SPISTATUS register (I/O address 1D9h) – This value selects 8 MHz SCLK speed, hardware IRQ disable, and left-shift data.
3. Write any value to SPIDATA2 (I/O address 1DCh) – This data will be ignored by the A/D converter.
4. Write the analog input channel number to bits 5-3 of SPIDATA3 (1DDh) – Any write operation to this register triggers an SPI transaction.
5. Poll the BUSY bit until the conversion is completed.
6. Read the conversion data from SPIDATA2 (lower 8 bits) and SPIDATA3 (upper 4 bits).

Each analog conversion returns the conversion data from the previous conversion. The first analog conversion after power-up or reset returns the data from ADCH0. The second conversion returns the conversion data from the channel addressed in the first conversion. Each successive conversion returns conversion data from the previous conversion.

This means that multiple conversions on the same A/D channel return valid data after every conversion, starting with the second conversion. However, if a different channel is selected between analog reads, two conversions will be necessary to return valid data from the new channel. The analog input code example on page 50 shows how to use a 32bit SPI frame for an automatic second conversion when only one sample is desired.

SPI Analog Input Code Example

The following code example illustrates the procedure for reading an analog voltage from the onboard ADC channel 3. A 32bit SPI frame is used to provide a valid single sample.

```
        MOV   DX, 1D8h
        MOV   AL, 35h     ;SPICONTROL: SPI Mode 00, 32bit, auto ADC_SS#
        OUT   DX, AL
        MOV   DX, 1D9h
        MOV   AL, 30h     ;SPISTATUS: 8MHz, no IRQ, left-shift
        OUT   DX, AL
                          ;SPIDATA2, SPIDATA1, SPIDATA0: don't care
        MOV   DX, 1DDh
        MOV   AL, 18h     ;SPIDATA3: ADC78H90 AIN4 = EBX-11 ADCH3
        OUT   DX, AL

BUSY:   MOV   DX, 1D9h    ;Get SPISTATUS
        IN    AL, DX
        AND   AL, 01h     ;Isolate the BUSY bit
        JNZ   BUSY        ;Loop back if SPI transaction not complete

        MOV   DX, 1DAh    ;Point to SPIDATA0 register
```

```
IN    AX, DX      ;16bit input reads current conversion data
                  ;from SPIDATA1 into AH and from SPIDATA0 into
                  ;AL
```

For more detailed information on the EBX-11 A/D converter, please refer to the National Semiconductor ADC78H90 Datasheet

ANALOG INPUT "BIT BANG" REGISTER

A special register is available at 1D5h that enables the direct control ("bit banging") of the ADC. To use this register, ADC field (bits D1-D0) of the MODCON register (1DFh) must be set to 0h (see Table 44 for mode control settings).

ADCBB (Read/Write) 1D5h

D7	D6	D5	D4	D3	D2	D1	D0
ADCIN	Reserved	Reserved	Reserved	Reserved	ADCCLK	ADCOUT	ADCCS0

Table 28: ADCBB Register Bit Assignments

Bit	Mnemonic	Description
D7	ADCIN	**Analog Input** – This bit is read only.
D6-D3	–	**Reserved** – These bits have no function.
D2	ADCCLK	**Analog Clock** – This bit is read/write.
D1	ADCOUT	**Analog Output** – This bit is read/write.
D0	ADCCS0	**Analog Chip Select** – This bit is read/write.

Digital I/O

The EBX-22 includes a 32-channel digital I/O interface. The digital lines are grouped into two banks of 16-bit bi-directional ports. The direction of each line is controlled by software. The digital I/O ports are powered up in the input mode. The 24 mA source/sink drive and short protected outputs are an excellent choice for industrial LVTTL interfacing. All I/O pins use 3.3V signaling.

Warning! Damage may occur if the I/O pins are connected to 5V logic.

Digital I/O can be controlled through the SPI interface or the digital I/O "bit bang" registers.

EXTERNAL CONNECTIONS

Digital I/O channels are available at connectors J15 and J23 as shown in Table 6 and Table 7, respectively.

DIGITAL I/O PORT CONFIGURATION USING THE SPI INTERFACE

Digital I/O channels 0-15 are accessed via SPI slave select 6 (writing 6h to the SS field of SPICONTROL). Channels 16-31 are accessed via SPI chip select 7 (writing 7h to the SS field). Each pair of I/O ports is configured by a set of paged I/O registers accessible through SPI. These registers control settings such as signal direction, input polarity, and interrupt source.

Digital I/O Interrupt Generation Using the SPI Interface

The EBX-22 digital I/O can be configured to issue hardware interrupts on the transition (high to low or low to high) of any digital I/O pin. IRQ assignment is made in SPI control register SPISTATUS. Note that this IRQ is shared among all SPI devices on-board and externally connected to the EBX-22. The IRQ is also shared with the PC/104 bus and must be enabled in CMOS for ISA IRQx. Digital I/O chip interrupt configuration is achieved through I/O port register settings. Please refer to the Microchip MCP23S17 datasheet for more information.

The on-board digital I/O chips must be configured for open-drain and mirrored interrupts in order for any SPI device to use hardware interrupts. The following code example illustrates how to do this. Normally, the BIOS initializes the on-board digital I/O chips at boot time.

```
      MOV   DX, 1D8h
      MOV   AL, 26h     ;SPICONTROL: SPI Mode 00, 24bit, auto DIO_0_SS#
      OUT   DX, AL
      MOV   DX, 1D9h
      MOV   AL, 30h     ;SPISTATUS: 8MHz, no IRQ, left-shift
      OUT   DX, AL
      MOV   DX, 1DBh
      MOV   AL, 44h     ;SPIDATA1: Mirror & Open-Drain interrupts
      OUT   DX, AL
      MOV   DX, 1DCh
      MOV   AL, 0Ah     ;SPIDATA2: MCP23S17 address 0x0A
      OUT   DX, AL
      MOV   DX, 1DDh
      MOV   AL, 40h     ;SPIDATA3: MCP23S17 write command
      OUT   DX, AL

BUSY: MOV   DX, 1D9h
      IN    AL, DX      ;Get SPI status
```

```
AND   AL, 01h     ;Isolate the BUSY bit
JNZ   BUSY        ;Loop back if SPI transaction is not complete

MOV   DX, 1D8h
MOV   AL, 27h     ;SPICONTROL: SPI Mode 00, 24bit, auto DIO_1_SS#
OUT   DX, AL
MOV   DX, 1D9h
MOV   AL, 30h     ;SPISTATUS: 8MHz, no IRQ, left-shift
OUT   DX, AL
MOV   DX, 1DBh
MOV   AL, 44h     ;SPIDATA1: Mirror & Open-Drain interrupts
OUT   DX, AL
MOV   DX, 1DCh
MOV   AL, 0Ah     ;SPIDATA2: MCP23S17 address 0x0A
OUT   DX, AL
MOV   DX, 1DDh
MOV   AL, 40h     ;SPIDATA3: MCP23S17 write command
OUT   DX, AL
```

Writing to a Digital I/O Port Using the SPI Interface

The following code example initiates a write of 55h to Digital I/O port bits DIO15-DIO8.

```
;Write 44h to configure MCP23S17 register IOCON

   MOV    DX, 1D8h
   MOV    AL, 26h       ;SPICONTROL: SPI Mode 00, 24bit, DIO_0_SS#
   OUT    DX, AL
   MOV    DX, 1D9h
   MOV    AL, 30h       ;SPISTATUS: 8MHz, no IRQ, left-shift
   OUT    DX, AL
   MOV    DX, 1DBh
   MOV    AL, 44h       ;SPIDATA1: mirror and open-drain interrupts
   OUT    DX, AL
   MOV    DX, 1DCh
   MOV    AL, 0Ah       ;SPIDATA2: MCP23S17 IOCON register address 0Ah
   OUT    DX, AL
   MOV    DX, 1DDh
   MOV    AL, 40h       ;SPIDATA3: MCP23S17 write command
   OUT    DX, AL
   CALL   BUSY          ;Poll busy flag to wait for SPI transaction

;Configure MCP23S17 register IODIRA for outputs

   MOV    DX, 1DBh
   MOV    AL, 00h       ;SPIDATA1: 00h for outputs
   OUT    DX, AL
   MOV    DX, 1DCh
   MOV    AL, 00h       ;SPIDATA2: MCP23S17 register address 00h
   OUT    DX, AL
   MOV    DX, 1DDh
   MOV    AL, 40h       ;SPIDATA3: MCP23S17 write command
   OUT    DX, AL
   CALL   BUSY          ;Poll busy flag to wait for SPI transaction

;Write 55h to MCP23S17 register GPIOA

   MOV    DX, 1DBh
   MOV    AL, 55h       ;SPIDATA1: data to write
   OUT    DX, AL
   MOV    DX, 1DCh
   MOV    AL, 14h       ;SPIDATA2: MCP23S17 register address 14h
   OUT    DX, AL
   MOV    DX, 1DDh
   MOV    AL, 40h       ;SPIDATA3: MCP23S17 write command
```

```
        OUT    DX, AL
        CALL   BUSY          ;Poll busy flag to wait for SPI transaction

BUSY:   MOV    DX, 1D9h
        IN     AL, DX        ;Get SPISTATUS
        AND    AL, 01h       ;Isolate the BUSY flag
        JNZ    BUSY          ;Loop if SPI transaction not complete
```

Reading a Digital I/O Port Using the SPI Interface

The following code example reads the DIO15-DIO8 input lines.

```
'REGISTER ASSIGNMENT
'--------------------
CONST SPICONTROL1 = &H1D8
CONST SPICONTROL2 = &H1D9
CONST SPISTATUS = &H1D9
CONST SPIDATA1 = &H1DB
CONST SPIDATA2 = &H1DC
CONST SPIDATA3 = &H1DD

'INITIALIZE EPM-22 SPI CONTROLLER
'================================

'EPM-22 SPICONTROL1 Register
'---------------------------
'D7 CPOL      = 0 SPI Clock Polarity (SCLK idles low)
'D6 CPHA      = 0 SPI Clock Phase (Data read on rising edge)
'D5 SPILEN1   = 1 SPI Frame Length (24-Bit)
'D4 SPILEN0   = 0  "    "     "       "
'D3 MAN_SS    = 0 SPI Slave Select Mode (Automatic)
'D2 SS2       = 1 SPI Slave Select (On-Board DIO 0-15)
'D1 SS1       = 1  "    "     "          "     "
'D0 SS0       = 0  "    "     "          "     "
OUT SPICONTROL1, &H26

'EPM-22 SPICONTROL2 Register
'---------------------------
'D7 IRQSEL1   = 0 IRQ Select (IRQ3)
'D6 IRQSEL0   = 0  "    "      "
'D5 SPICLK1   = 1 SPI SCLK Frequency (8.333 MHz)
'D4 SPICLK0   = 1  "    "      "          "
'D3 HW_IRQ_EN = 0 Hardware IRQ Enable (Disabled)
'D2 LSBIT_1ST = 0 SPI Shift Direction (Left Shifted)
'D1 0         = 0 This bit has no function
'D0 0         = 0 This bit has no function
OUT SPICONTROL2, &H30


'INITIALIZE MCP23S17
'===================

'MCP23S17 IOCON Register
'-----------------------
'D7 BANK      = 0 Registers in same bank (addresses are sequential)
'D6 MIRROR    = 1 The INT pins are internally connected
'D5 SEQOP     = 0 Sequential op disabled. Addr ptr does not increment.
'D4 DISSLW    = 0 Slew rate control for SDA output (enabled)
'D3 HAEN      = 0 Hardware address enable (addr pins disabled)
'D2 ODR       = 1 INT pin is open-drain
'D1 INTPOL    = 0 Polarity of INT output pin (ignored when ODR=1)
'D0 0         = 0 This bit has no function
OUT SPIDATA1, &H44

'MCP23S17 IOCON Register Address
'-------------------------------
OUT SPIDATA2, &HA
```

```
'MCP23S17 SPI Control Byte (Write)
'--------------------------------
'D7 SLAVEFA3  = 0 Slave Address (Fixed Portion)
'D6 SLAVEFA2  = 1   "       "       "     "
'D5 SLAVEFA1  = 0   "       "       "     "
'D4 SLAVEFA0  = 0   "       "       "     "
'D3 SLAVEHA2  = 0 Slave Address Bits (Hardware Address Bits)
'D2 SLAVEHA1  = 0   "       "       "     "
'D1 SLAVEHA0  = 0   "       "       "     "
'D0 READWRITE = 0 Read/Write Bit = Write
OUT SPIDATA3, &H40

WHILE (INP(SPISTATUS) AND &H1) = &H1: WEND

'INITIALIZE DIRECTION OF DIO LINES D15-D8 AS INPUTS
'=================================================

'Direction = All Inputs
OUT SPIDATA1, &HFF

'MCP23S17 IODIRA Register Address
OUT SPIDATA2, &H0

'MCP23S17 SPI Control Byte (Write)
OUT SPIDATA3, &H40

WHILE (INP(SPISTATUS) AND &H1) = &H1: WEND

'Repeat until ESC key is pressed
WHILE INKEY$ <> CHR$(27)


  'READ DIO INPUT DATA FROM MCP23S17
  '---------------------------------

  'MCP23S17 GPIOA Register Address
  OUT SPIDATA2, &H12

  'MCP23S17 SPI Control Byte (Read)
  OUT SPIDATA3, &H41

  WHILE (INP(SPISTATUS) AND &H1) = &H1: WEND

  'DIO Input Data
  PRINT HEX$(INP(SPIDATA1))

WEND

SYSTEM
```

DIGITAL I/O "BIT BANG" REGISTER

A special register is available at 1D6h, which enables the direct control ("bit banging") of digital I/O. To use this register, the DIO field (bits D4-D3) of the MODCON register (1DFh) must be set to 0h (see Table 44 for mode control settings).

DIOBB (Read/Write) 1D6h

D7	D6	D5	D4	D3	D2	D1	D0
DIOIN	DIOINT	Reserved	Reserved	DIOCLK	DIOOUT	DIOCS1	DIOCS0

Table 29: DIOBB Register Bit Assignments

Bit	Mnemonic	Description
D7	DIOIN	**Digital I/O Input** – This bit is read-only.
D6	DIOINT	**Digital I/O Interrupt** – This bit is read-only.
D5-D4	–	**Reserved** – These bits have no function.
D3	DIOCLK	**Digital I/O Clock** – This bit is read/write.
D2	DIOOUT	**Digital I/O Output** – This bit is read/write.
D1-D0	DIOCS	**Digital I/O Chip Select** – These bits are read/write.

SPI Interface

The serial peripheral interface (SPI) can function in two modes on the EBX-22. In legacy mode, the interface functions as implemented in other VersaLogic SBCs, such as the EBX-11 Rev. 6.00 and above, and makes use of a set of control and data registers. In “bit bang” mode, you can operate the SPIBB register (1D7h) directly. Each mode is described in this section.

SPI is, in its simplest form, a three wire serial bus. One signal is a Clock, driven only by the permanent Master device on-board. The others are Data In and Data Out with respect to the Master. The VersaLogic SPI implementation adds additional features, such as chip selects and an interrupt input to the Master. The Master device initiates all SPI transactions. A slave device responds when its Chip Select is asserted and it receives Clock pulses from the Master.

The SPI clock rate can be software configured to operate at speeds between 1 MHz and 8 MHz. Please note that since this clock is divided from a 33 MHz PCI clock, the actual generated frequencies are not discrete integer MHz frequencies. All four common SPI modes are supported through the use of clock polarity and clock idle state controls.

EXTERNAL CONNECTIONS

Up to four serial peripheral interface (SPI) devices can be attached to the EBX-22 at connector J25 using the CBR-1401 or CBR-1402 cable. The interface provides the standard SPI signals: SCLK (Serial Clock), MISO (Master In Slave Out), and MOSI (Master Out Slave In), as well as four chip selects, SS0# to SS3#, and an Interrupt Input, SINT#.

Table 30: SPI Expansion Bus Pinout

J25 Pin	Signal Name	Function
1	V5_0	+5.0V (Protected)
2	SCLK	Serial Clock
3	GND	Ground
4	MISO	Serial Data In
5	GND	Ground
6	MOSI	Serial Data Out
7	GND	Ground
8	SS0#	Chip Select 0
9	SS1#	Chip Select 1
10	SS2#	Chip Select 2
11	SS3#	Chip Select 3
12	GND	Ground
13	SINT#	Interrupt Input
14	V5_0	+5.0V (Protected)

SPI LEGACY MODE

The following tables describe the legacy SPI control registers (SPICONTROL and SPISTATUS) and data registers (SPIDATA3-0), such as those used on the EBX-11. To enable SPI legacy mode, the SPI field (bits D6-D5) of the MODCON register (1DFh) must be set to 1h.

SPICONTROL (READ/WRITE) 1D8h

D7	D6	D5	D4	D3	D2	D1	D0
CPOL	CPHA	SPILEN1	SPILEN0	MAN_SS	SS2	SS1	SS0

Table 31: SPI Control Register 1 Bit Assignments

Bit	Mnemonic	Description
D7	CPOL	**SPI Clock Polarity –** Sets the SCLK idle state. 0 = SCLK idles low 1 = SCLK idles high
D6	CPHA	**SPI Clock Phase –** Sets the SCLK edge on which valid data will be read. 0 = Data read on rising edge 1 = Data read on falling edge
D5-D4	SPILEN	**SPI Frame Length –** Sets the SPI frame length. This selection works in manual and auto slave select modes. **SPILEN1 SPILEN0 Frame Length** 0 0 8-bit 0 1 16-bit 1 0 24-bit 1 1 32-bit
D3	MAN_SS	**SPI Manual Slave Select Mode –** This bit determines whether the slave select lines are controlled through the user software or are automatically controlled by a write operation to SPIDATA3 (1DDh). If MAN_SS = 0, then the slave select operates automatically; if MAN_SS = 1, then the slave select line is controlled manually through SPICONTROL bits SS2, SS1, and SS0. 0 = Automatic, default 1 = Manual
D2-D0	SS	**SPI Slave Select –** These bits select which slave select will be asserted. The SSx# pin on the base board will be directly controlled by these bits when MAN_SS = 1. **SS2 SS1 SS0 Slave Select** 0 0 0 None, port disabled 0 0 1 SPX Slave Select 0, J17 pin-8 0 1 0 SPX Slave Select 1, J17 pin-9 0 1 1 SPX Slave Select 2, J17 pin-10 1 0 0 SPX Slave Select 3, J17 pin-11 1 0 1 On-Board A/D Converter Slave Select 1 1 0 On-Board Digital I/O Ch 0-Ch 15 Slave Select 1 1 1 On-Board Digital I/O Ch 16-Ch 31 Slave Select

SPISTATUS (READ/WRITE) 1D9h

D7	D6	D5	D4	D3	D2	D1	D0
IRQSEL1	IRQSEL0	SPICLK1	SPICLK0	HW_IRQ_EN	LSBIT_1ST	HW_INT	BUSY

Table 32: SPI Control Register 2 Bit assignments

Bit	Mnemonic	Description
D7-D6	IRQSEL	**IRQ Select** – These bits select which IRQ will be asserted when a hardware interrupt from a connected SPI device occurs. The HW_IRQ_EN bit must be set to enable SPI IRQ functionality. **IRQSEL1 IRQSEL0 IRQ** 0 0 IRQ3 0 1 IRQ4 1 0 IRQ5 1 1 IRQ10 **Note:** The on-board digital I/O chips must be configured for open-drain and mirrored interrupts in order for any SPI device to use hardware interrupts.
D5-D4	SPICLK	**SPI SCLK Frequency –** These bits set the SPI clock frequency. **SPICLK1 SPICLK0 Frequency** 0 0 1.042 MHz 0 1 2.083 MHz 1 0 4.167 MHz 1 1 8.333 MHz
D3	HW_IRQ_EN	**Hardware IRQ Enable** – Enables or disables the use of the selected IRQ (IRQSEL) by an SPI device. 0 = SPI IRQ disabled, default 1 = SPI IRQ enabled **Note:** The selected IRQ is shared with PC/104 ISA bus devices. CMOS settings must be configured for the desired ISA IRQ.
D2	LSBIT_1ST	**SPI Shift Direction** – Controls the SPI shift direction of the SPIDATA registers. The direction can be shifted toward the least significant bit or the most significant bit. 0 = SPIDATA data is left-shifted (MSbit first), default 1 = SPIDATA data is right-shifted (LSbit first)
D1	HW_INT	**SPI Device Interrupt State –** This bit is a status flag that indicates when the hardware SPX signal SINT# is asserted. 0 = Hardware interrupt on SINT# is deasserted 1 = Interrupt is present on SINT# This bit is read-only and is cleared when the SPI device's interrupt is cleared.
D0	BUSY	**SPI Busy Flag** – This bit is a status flag that indicates when an SPI transaction is underway. 0 = SPI bus idle 1 = SCLK is clocking data in and out of the SPIDATA registers This bit is read-only.

SPIDATA0 (READ/WRITE) 1DAh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA1 (READ/WRITE) 1DBh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA2 (READ/WRITE) 1DCh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA3 (READ/WRITE) 1DDh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA3 contains the most significant byte (MSB) of the SPI data word. A write to this register will initiate the SPI clock and, if the MAN_SS bit = 0, will also assert a slave select to begin an SPI bus transaction. Increasing frame sizes from 8-bit use the lowest address for the least significant byte of the SPI data word; for example, the LSB of a 24-bit frame would be SPIDATA1. Data is sent according to the LSBIT_1ST setting. When LSBIT_1ST = 0, the MSbit of SPIDATA3 is sent first, and received data will be shifted into the LSbit of the selected frame size set in the SPILEN field. When LSBIT_1ST = 1, the LSbit of the selected frame size is sent first, and the received data will be shifted into the MSbit of SPIDATA3.

SPI "BIT BANG" MODE

A special register is available at 1D7h, which enables the direct control ("bit banging") of the SPI interface. To use this register, the SPI field (bits D6-D5) of the MODCON register (1DFh) must be set to 0h (see Table 44 for mode control settings).

SPIBB (Read/Write) 1D7h

D7	D6	D5	D4	D3	D2	D1	D0
SPI_IN	SPI_INT	SPI_CLK	SPI_OUT	SPI_CS3	SPI_CS2	SPI_CS1	SPI_CS0

Table 33: SPIBB Bit Assignments

Bit	Mnemonic	Description
D7	SPI_IN	**SPI Input** – This bit is read-only.
D6	SPI_INT	**SPI Interrupt** – This bit is read-only.
D5	SPI_CLK	**SPI Clock** – This bit is read/write.
D4	SPI_OUT	**SPI Output** – This bit is read/write.
D3-D0	SPI_CS	**SPI Chip Select** – These bits are read/write.

PWM Outputs and TACH Inputs

The EBX-22 incorporates three pulse width modulation (PWM) outputs and three tachometer (TACH) inputs which can be used, in a limited fashion, as general purpose frequency generators and counter/timers.

The PWM output frequency options are: 11.0 Hz, 14.6 Hz, 21.9 Hz, 29.3 Hz, 35.2 Hz, 44.0 Hz, 58.6 Hz, 87.7 Hz, 15 kHz, 20 kHz, 25 kHz, and 30 kHz. The PWM duty cycle is user definable from 0% (1/256) to 100% (255/256) and also invertible.

The SCH3114 Super I/O chip includes a fan speed monitoring feature, which uses TACH inputs. When the TACHs are set to manual mode, the inputs can be used as counter/timers instead of for fan speed monitoring. By default, the 16-bit tachometer registers hold the number of 90 kHz pulses that occur within five tachometer input edge-transitions (for example, two TACH pulses).

In manual mode, the tachometer circuit begins monitoring the TACH inputs on the 1st edge detected and continues counting until the last edge is detected. If the counter overflows before the number of edges is detected, it sets the count to FFFFh. If no edges are detected, a “stalled-fan event” occurs and the counter is set to FFFFh.

Refer to the SMSC SCH3114 Super I/O datasheet for more information and detailed register descriptions.

External Connections

Table 34: TAC and PWM Pinout

J15 Pin	Signal	CBR-4004 Connector	CBR-4004 Pin (Signal)
1	TAC_IN 1	**J1 TAC Input Purpose I/O**	5 (IO1)
2	TAC_IN 2		4 (IO2)
3	TAC_IN 3		3 (IO3)
4	PLD_CLK		2 (IO4)
5	GND		1 (GND1)
6	PWM_OUT1	**J2 PWM Output**	5 (IO5)
7	PWM_OUT2		4 (IO6)
8	PWM_OUT3		3 (IO7)
9	NC		2 (IO8)
10	GND		1 (GND1)

PWM Output and Tach Input Code Example

The following code provides guidelines for using PWM outputs and tachometer inputs as general purpose timers. Some steps are designated as required, but all steps are recommended.

```
;Controlling PWM outputs manually

;Pause the SCH3114 Hardware Monitor (optional)
MOV     DX, C70h    ;Hardware Monitor index port
MOV     AL, 40h     ;Ready,Lock,Start Register
OUT     DX, AL
MOV     DX, C71h    ;Hardware Monitor data port
IN      AL, DX      ;Read Current Value
AND     AL, FEh     ;Disable Start bit
OUT     DX, AL

;Set PWMs to manual mode (required)
```

```
;       PWM 1 Configuration Register = 5Ch
;       PWM 2 Configuration Register = 5Dh
;       PWM 3 Configuration Register = 5Eh
;
MOV     DX, C70h
MOV     AL, 5Ch     ;PWM 1 Configuration Register
OUT     DX, AL
MOV     DX, C71h
IN      AL, DX      ;Read Current Value
OR      AL, E0h     ;Set Manual Mode
OUT     DX, AL

;Set Zone X Low Temp Limits to valid values (Required)
;All three must be set even if only one PWM is used...
MOV     DX, C70h
MOV     AL, 67h     ;Zone 1 Low Temp Limit Register
OUT     DX, AL
MOV     DX, C71h
MOV     AL, 81h     ;any value other than default of 80h
OUT     DX, AL

MOV     DX, C70h
MOV     AL, 68h     ;Zone 2 Low Temp Limit Register
OUT     DX, AL
MOV     DX, C71h
MOV     AL, 81h     ;Any value other than default of 80h
OUT     DX, AL

MOV     DX, C70h
MOV     AL, 69h     ;Zone 3 Low Temp Limit Register
OUT     DX, AL
MOV     DX, C71h
MOV     AL, 81h     ;Any value other than default of 80h
OUT     DX, AL

;Set PWM current duty cycle (optional)
;       PWM 1 Current Duty Cycle Register = 30h
;       PWM 2 Current Duty Cycle Register = 31h
;       PWM 3 Current Duty Cycle Register = 32h
;
MOV     DX, C70h
MOV     AL, 30h     ;PWM 1 Current Duty Cycle Register
OUT     DX, AL
MOV     DX, C71h
MOV     AL, 80h     ;50% Duty Cycle, 40h = 25%, etc.
OUT     DX, AL

;Set PWM Frequency (optional)
;       Zone 1 Range/PWM 1 Frequency Register = 5Fh
;       Zone 2 Range/PWM 2 Frequency Register = 60h
;       Zone 3 Range/PWM 3 Frequency Register = 61h
;
;       Frequency = low nibble
;       X0 = 11.0 Hz       X6 = 58.6Hz
;       X1 = 14.6Hz        X7 = 87.7Hz
;       X2 = 21.9Hz        X8 = 15 KHz
;       X3 = 29.3Hz        X9 = 20 KHz
;       X4 = 35.2Hz        XA = 30 KHz
;       X5 = 44.0Hz        XB = 25 KHz (default)
;
MOV     DX, C70h
MOV     AL, 5Fh     ;Zone 1 Range/PWM 1 Frequency
```

```
OUT     DX, AL
MOV     DX, C71h
IN      AL, DX      ;Read Current Value
AND     AL, F1h     ;Set to 14.6 Hz
OUT     DX, AL

;Re-start the SCH3114 Hardware Monitor (required)
MOV     DX, C70h    ;Hardware Monitor index port
MOV     AL, 40h     ;Ready,Lock,Start Register
OUT     DX, AL
MOV     DX, C71h    ;Hardware Monitor data port
IN      AL, DX      ;Read Current Value
OR      AL, 1h      ;Enable Start bit
OUT     DX, AL

;Reading FanTachs

;Read FanTach LSB first then read the latched MSB
;       fantach 1 LSB = 28h
;       fantach 1 MSB = 29h
;       fantach 2 LSB = 2Ah
;       fantach 2 MSB = 2Bh
;       fantach 3 LSB = 2Ch
;       fantach 3 MSB = 2Dh
;
MOV     DX, C70h
MOV     AL, 28h     ;FanTach 1 LSB
OUT     DX, AL
MOV     DX, C71h
IN      BL, DX
MOV     DX, C70h
MOV     AL, 29h     ;FanTach 1 MSB
IN      BH, DX

;BX now contains 16-bit number of 90KHz pulses that
;were counted within 5 edges (2 pulses) of the tach input.
;Input Frequency f = 1 / (BX * 11.11uS / 2), RPMs = f * 60
```

PC/104 Expansion Bus

EBX-22 has limited support of the PC/104 bus. Most PC/104 cards will work, but be sure to check the requirements of your PC/104 card against the list below.

PC/104 I/O SUPPORT

The ISA I/O ranges listed below are supported. The I/O ranges allocated to COM ports 1-4 are available to ISA when the on-board COM port function is disabled in CMOS Setup.

- 080h
  200h – 2EFh
  2F8h – 36Fh
  3E8h – 3EFh
  3F8h – 3FFh
- Available base I/O addresses for COM ports are: 220h, 228h, 238h, 338h, 3F8h, 2F8h, 3E8h, and 2E8h.

PC/104 MEMORY SUPPORT

Memory ranges supported:

- D0000h-DFFFFh, 8 and 16-bit transfers

IRQ SUPPORT

The following IRQs are available on the PC/104 bus:

- IRQ 3, IRQ 4, IRQ5, and IRQ 10

Each of the four IRQs must be enabled in CMOS Setup before they can be used on the ISA bus. Because ISA IRQ sharing is not supported, make sure that any IRQ channel used for an ISA device is not used elsewhere. For example, if ISA IRQ 4 is enabled, you must use a different IRQ for COM1.

DMA SUPPORT

The current revision of the board does not support PC/104 DMA.

Memory Map

The lower 1 MB memory map of the EBX-22 is arranged as shown in the following table.

Table 35: Memory Map

Start Address	End Address	Comment
E0000h	FFFFFh	System BIOS
D0000h	DFFFFh	PCI or ISA BIOS extensions or boot ROMS
C0000h	CFFFFh	Video BIOS
A0000h	BFFFFh	Video RAM
00000h	9FFFFh	System RAM

I/O Map

The following table lists the common I/O devices in the EBX-22 I/O map. User I/O devices should be added with care to avoid the devices already in the map shown in below.

Table 36: I/O Map

I/O Device	Standard I/O Addresses
Reserved	1B0h – 1BFh
ADC Data Registers	1C0h – 1CFh
PLED and Product ID Register	1D0h
Revision and Type Register	1D1h
Video BIOS Select Register	1D2h
Reserved	1D3h
GPO	1D4h
ADC, DIO, SPI Bit Bang Registers	1D5h – 1D7h
Legacy SPI interface	1D8h – 1DDh
IRQ, Resource ISA Enable Registers	1DEh
SPI, DIO, ADC Mode Register	1DFh
Watchdog Timer	1E0h – 1E3h
Primary Hard Drive Controller	1F0h – 1F7h
COM4 Serial Port	2E8h – 2EFh
LPT1 Parallel Port	378h – 37Fh
COM3 Serial Port	3E8h – 3EFh
COM2 Serial Port	2F8h – 2FFh
COM1 Serial Port	3F8h – 3FFh

Note The I/O ports occupied by on-board devices are freed up when the device is disabled in CMOS Setup. This does not apply to SPI and reserved registers.

Interrupt Configuration

The EBX-22 has the standard complement of PC type interrupts. Four non-shared interrupts are routed to the PC/104 bus, and up to four IRQ lines can be allocated as needed to PCI devices. The following tables show the default and allowed interrupt settings. There are no interrupt configuration jumpers. All configuration is handled through CMOS Setup. If your design needs to use interrupt lines on the PC/104 bus, IRQ5 and IRQ10 are recommended. (IRQ3 and IRQ4 are normally used by COM ports on the main board.) COM ports can share interrupts with other COM ports, but not with other devices.

Table 37: EBX-22 IRQ Settings

● = default setting O = allowed setting

Source	IRQ															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer 0	●															
Keyboard		●														
Slave PIC			●													
COM1				O	●	O		O								
COM2				●	O	O		O								
COM3				O	O	O		O								
COM4				O	O	O		O								
Floppy							●									
LPT1*						O		●								
RTC									●							
Mouse													●			
Math Chip														●		
IDE SATA															●	
IDE PATA																●
ISA IRQ10											O					
ISA IRQ3				O												
ISA IRQ4					O											
ISA IRQ5						O										
PCI INTA#						O				O	O	●				
PCI INTB#						O				O	O	●				
PCI INTC#						O				O	O	●				
PCI INTD#						O				●	O	O				

* When LPT1 is in floppy disk mode, the pins change function, the LPT device is no longer available, and the floppy disk controller uses IRQ 6.

Table 38: PCI Interrupt Settings

● = default setting O = allowed setting

Source	PCI Interrupt			
	INTA#	INTB#	INTC#	INTD#
Video	●			
Audio		●		
USB 1.1	●			
USB 1.1		●		
USB 1.1			●	
USB 2.0				●
Ethernet0			●	
Ethernet1				●

Product ID and PLED Register

PRODID (Read/Write) 1D0h

D7	D6	D5	D4	D3	D2	D1	D0
PLED	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Table 39: PRODID Register Bit Assignments

Bit	Mnemonic	Description
D7	PLED	**Light Emitting Diode** – Controls the programmable LED on connector J4. 0 = Turns LED off 1 = Turns LED on
D6-D0	ID	**Product ID –** These bits are hard-coded to represent the product ID. **ID6 ID5 ID4 ID3 ID2 ID1 ID0 Product ID** 0 0 0 0 0 1 0 EBX-22 These bits are read-only.

Revision and Type Register

REVTYP (Read Only) 1D1h

D7	D6	D5	D4	D3	D2	D1	D0
PLDREV4	PLDREV3	PLDREV2	PLDREV1	PLDREV0	EXTEMP	PLDCUST	PLDDEV

This register is used to indicate the PLD revision level and model of the EBX-22.

Table 40: REVTYP Register Bit Assignments

Bit	Mnemonic	Description
D7-D3	PLDREV	**PLD Revision Level** – These bits represent the EBX-22 PLD revision level. **Bit 4 / Bit 3 / Bit 2 / Bit 1 / Bit 0 / PLD Revision Level** 0 0 0 0 1 — 2.01 0 0 0 1 0 — 3.00 These bits are read-only.
D2	EXTEMP	**Extended Temperature** – This bit indicates whether the EBX-22 is an extended temperature model. 0 = Standard temperature range model 1 = Extended temperature range model This bit is read-only.
D1	PLDCUST	**Custom PLD** – This bit indicates whether the EBX-22 has a custom PLD. 0 = Standard PLD 1 = Custom PLD This bit is read-only.
D0	PLDDEV	**PLD in Development** – This bit indicates whether the EBX-22 PLD is in development. 0 = PLD not in development 1 = PLD in development This bit is read-only.

Jumper Status Register

JSR (Read Only) 1D2h

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VB_SEL	Reserved

Table 41: JSR Register Bit Assignments

Bit	Mnemonic	Description
D7-D2	–	**Reserved** – These bits have no function.
D1	VB_SEL	**Video BIOS Selection –** Indicates the status of jumper V6[3-4]. 0 = Jumper in, Primary Video BIOS selected 1 = Jumper out, Secondary Video BIOS selected This bit is read-only.
D0	–	**Reserved** – This bit has no function.

General Purpose Output Register

GPO (Read/Write) 1D4h

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	GPO2	GPO1	GPO0

This register is used for general purpose outputs.

Table 42: GPO Register Bit Assignments

Bit	Mnemonic	Description
D7-D3	–	**Reserved** – These bits have no function.
D2-D0	GPO	**General Purpose Outputs**

IRQ and Resource ISA Routing Register

IRQISA (Read/Write) 1DEh

D7	D6	D5	D4	D3	D2	D1	D0
COM2	COM1	COM4	COM3	IRQ10	IRQ5	IRQ4	IRQ3

This register is used to allow IRQs to be routed across the ISA bridge.

Table 43: IRQISA Register Bit Assignments

Bit	Mnemonic	Description
D7	COM2	**COM2 I/O** 0 = I/O range for COM2 is used for on-board UART 1 = I/O range for COM2 is forwarded to ISA bus for use by expansion cards
D6	COM1	**COM1 I/O** 0 = I/O range for COM1 is used for on-board UART 1 = I/O range for COM1 is forwarded to ISA bus for use by expansion cards
D5	COM4	**COM4 I/O** 0 = I/O range for COM4 is used for on-board UART 1 = I/O range for COM4 is forwarded to ISA bus for use by expansion cards
D4	COM3	**COM3 I/O** 0 = I/O range for COM3 is used for on-board UART 1 = I/O range for COM3 is forwarded to ISA bus for use by expansion cards
D3	IRQ10	**IRQ10** 0 = IRQ10 on PC/104 (ISA) bus is ignored 1 = ISA bridge forwards IRQ10 to host
D2	IRQ5	**IRQ5** 0 = IRQ5 on PC/104 (ISA) bus is ignored 1 = ISA bridge forwards IRQ5 to host
D1	IRQ4	**IRQ4** 0 = IRQ4 on PC/104 (ISA) bus is ignored 1 = ISA bridge forwards IRQ4 to host
D0	IRQ3	**IRQ3** 0 = IRQ3 on PC/104 (ISA) bus is ignored 1 = ISA bridge forwards IRQ3 to host

Mode Control Register

MODCON (Read/Write) 1DFh

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	SPI1	SPI0	DIO1	DIO0	Reserved	ADC1	ADC0

This register is used to set the mode of the analog input, digital I/O, and SPI interfaces.

Table 44: MODCON Register Bit Assignments

Bit	Mnemonic	Description
D7	–	**Reserved** – This bit has no function.
D6-D5	SPI	**SPI Mode Control** – These bits set the mode of the general purpose I/O function. **D6 D5 Mode** 0 0 Use register 1D7h to “bit bang” individual bits. 0 1 Legacy EBX-11 SPI interface using registers 1D8h-1DDh (reset default). 1 0 Reserved – do not use. 1 1 Reserved – do not use.
D4-D3	DIO	**DIO Mode Control** – These bits set the mode of the digital I/O function. **D4 D3 Mode** 0 0 Use register 1D6h to “bit bang” individual bits. 0 1 Legacy EBX-11 SPI interface using registers 1D8h-1DDh (reset default). 1 0 Reserved – do not use. 1 1 Reserved – do not use.
D2	–	**Reserved** – This bit has no function.
D1-D0	ADC	**Analog Input Mode Control** – These bits set the mode of the analog input function. **D1 D0 Mode** 0 0 Use register 1D5h to “bit bang” individual bits. 0 1 Legacy EBX-11 SPI interface using registers 1D8h-1DDh (reset default). 1 0 ADC state machine continuously updates eight 16-bit registers. 1 1 Reserved – do not use.

Appendix A – References

CPU VIA Eden	VIA Eden Datasheet
Chipset VIA CX700	CX700 Datasheet
Ethernet Controller Intel 82551ER	Intel Corporation
PC/104 Specification *PC/104 Resource Guide*	PC/104 Consortium
PC/104-*Plus* Specification *PC/104 Resource Guide*	VersaLogic Corporation
General PC Documentation *The Programmer's PC Sourcebook*	Microsoft Press
General PC Documentation *The Undocumented PC*	Powell's Books